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Development of a Distributed Digital Array Radar (DDAR)

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MONTEREY, CALIFORNIA

THESIS

DEVELOPMENT OF A DISTRIBUTED DIGITAL ARRAY RADAR (DDAR)

by

Pontus Djerf
Ioannis Tornazakis

September 2008

Thesis Advisor:	David Jenn
Second Reader:	Robert Broadston

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Other issues addressed in the research include a comprehensive investigation of the demodulator performance, and the development of Controller and processing software in LabVIEW.

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DEVELOPMENT OF A DISTRIBUTED DIGITAL ARRAY RADAR (DDAR)

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Distributed digital arrays have many potential applications in radar and communication systems. The objective of this thesis is to re-examine previous research on distributed digital array radar (DDAR) and evaluate several critical aspects of a proposed wireless architecture. Self-standing transmit/receive (T/R) modules are synchronized wirelessly. An important issue addressed in this thesis is whether a simple low-cost synchronization circuit would perform adequately. To this end two breadboard T/R modules were built to support test and evaluation. Both measurements and simulations were performed.

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I. INTRODUCTION

A. BACKGROUND

In a time when the threats are no longer just from unfriendly states, a missile attack can be launched virtually from everywhere. Furthermore, today's Intercontinental Ballistic Missiles (ICBM) can have ranges up to 5500 kilometers [1]. To counter these kinds of threats, robust radar platforms must be designed and deployed. Modern warships can serve as ballistic missile defense (BMD) platforms because they are both mobile and can carry a variety of sensors and weapons.

The long-range missile detection capability of the U.S. Navy is provided by the Ticonderoga (CG 47) and Arleigh Burke (DDG 51)-class warships (see Figure 1). Those ships have the AN/SPY-1 radar system. It is mounted on the superstructure of the ship with phased array panels facing in four different directions to get a total coverage of 360 degrees. The radar operates in the S-band and its maximum detection range capability is estimated to 370 kilometers [2]. For BMD that detection range is deemed insufficient.

Figure 1. CG 56 (left) and DDG 51 (right) both equipped with the AN/SPY-1 system (From [3])

Future Navy planning includes the next generation destroyers, the Zumwalt-class DDG 1000 (see Figure 2). This lead ship is scheduled to be delivered in 2012 [4]. The ship will be equipped with a dual band radar system. On one hand, the Volume Search

Radar (VSR) will operate in the L-band; on the other, the AN/SPY-3 Multi Function Radar (MFR) will work in the X-band. This system will provide increased performance in both detection and targeting compared to the AN/SPY-1.

Figure 2. DDG 1000 with the dual band radar system (From [5])

One limiting factor with the above systems is the size of the phased array antennas. To further increase the angular resolution larger arrays are needed. This can be accomplished if you can use the ship's whole structure. The Radar Cross Section (RCS) of the ship is also adversely affected by the need for mounting the large antenna arrays. As a solution to these problems an array system with distributed elements integrated into the ship's hull, as shown in Figure 3, would comprise a larger distributed antenna and thus high angular resolution.

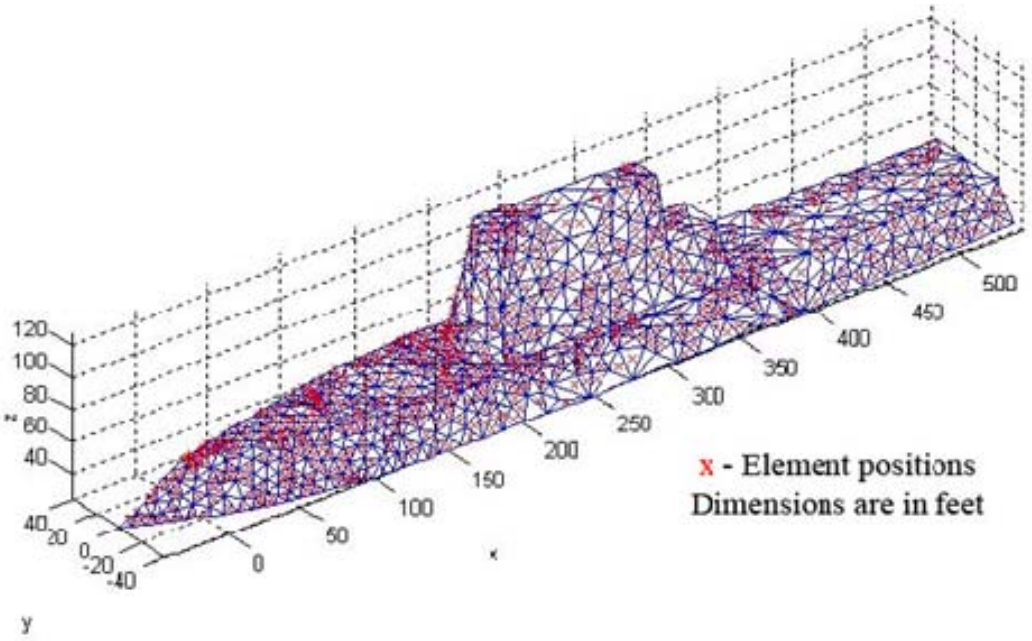

Figure 3. CAD model of Zumwalt-class sized ship with 1,200 randomly distributed integrated antenna elements (From [6])

The Office of Naval Research (ONR) sponsored a NPS project to improve ship-based radar performance and antenna integration. The goal of the project was to design an integrated phased array radar capable of long-range detection. An important component is the "aperstructure" design philosophy. The main idea is to use one central Digital Beamformer and Controller (computer) and distributed T/R modules with array elements integrated into the ship's hull or superstructure. Furthermore, data transfer between the modules and Controller is done by a wireless network. A basic block diagram of the array architecture is shown in Figure 4. A critical function supported by the computer controller is frequency/phase synchronization and timing.

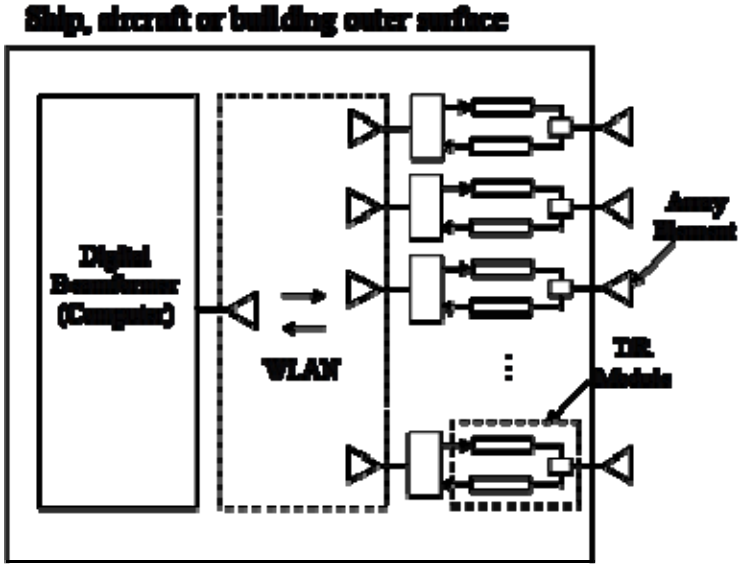

Figure 4. Wirelessly networked digital phased array architecture (From [7])

As already mentioned, the array elements are integrated into the ship's hull. This has to be done early in the ship's construction phase. The only cable connection between the element's T/R module and the hull will be the power supply. The benefits will include, lower RCS due to the lack of a large antenna array, higher survivability and sustainability because if damage is caused to some of the T/R modules the system can still operate. Furthermore, there is no single point of failure compared to an ordinary array antenna. Finally, the T/R modules can be hot-swapped if a failure occurs. Due to the digital nature of the array it can be reconfigured for multiple functions.

B. PREVIOUS WORK

Several students at NPS have contributed to the Distributed Digital Array Radar (DDAR) project.[1] The contributions from previous work are summarized below.

Tong [6] built a Computer-Aided Design (CAD) model to evaluate the theoretical detection range for a DD(X)-sized ship. In his model he used the ship structure and

[1] In previous years the name of the project was Wirelessly Networked Aperstructure Digital Phased Array (WNADPA).

distributed a various number of antennas all over the ship. After this he used a MATLAB program to plot both the beam pattern and the main lobe gain. Further work was done to estimate the number of elements needed to achieve a detection range of 1000 km. The performance of the simulated array was plotted versus the number of elements used and Tong found out that approximately 400 elements were needed to achieve the desired detection range. Later in his work he designed and simulated a U-slot antenna for integration into the ship structure. The antenna electrical characteristics were determined.

Yong [8] worked with the modulator and demodulator boards that are used for critical concept demonstration of the DDAR project. He evaluated the linear relationship between these two components. He verified that there is a linear relationship between the transmitted phase from the modulator board and the received phase from the demodulator board. After this Yong continued his work with evaluating the possibility of distributing both control signals and LO signals to the antenna element wirelessly. His test results verified that it would be possible.

Loke [9] showed that wireless synchronization for the T/R Modules using each element in turn was effective and easily implemented in the hardware. This implementation was chosen for the demonstration array because of its simplicity even though the method is inefficient. Another contribution from Loke is his work with the problem of synchronizing T/R modules on a platform that has deforming surfaces. His conclusion was that no correction is needed on radar that is operating in the VHF/UHF frequency bands because ship deformation is small compared to the wavelength.

Burgstaller [10] measured all scattering parameters for the hardware used in the demonstration array T/R modules. The measured parameters were then compared and verified to the different manufactures specifications. After the verification was done, Burgstaller integrated the components into a demonstration T/R module. Using MATLAB and CST Microwave Studio, an eight element linear array was simulated.

Yeo [11] worked on designing of the user interface for the DDAR control, and the development of the T/R modules together with Burgstaller. He also manufactured all the cables that were needed for the demonstration setup. When the modules were completed,

they performed several measurements to verify the performance of the T/R modules. One goal of the measurements was to find out if there was any interference between the modulator and the demodulator during operation. Their conclusions were that the module worked properly without any observable interference between the modulator and the demodulator.

Grahn [12] continued working with the DDAR project and his challenge was to design and evaluate a synchronization process for the T/R modules. He designed a synchronization circuit, using Commercial-off-the-Shelf (COTS) hardware and implemented the circuit into the two existing T/R Modules. The result of several measurements showed that the synchronization circuit works properly in "wired" mode. The result from the wireless mode measurements indicated that more work is needed before the synchronization circuit works properly. Problems occurred with the Power Amplifier (LPA), which injected an unpredictable phase shift into the system. Furthermore, significant LO leakage through the circulator was found.

Noris [13] focused on the wireless networking of the full scale radar system. He also analyzed the existing wireless technologies and guided transmission media. Furthermore, he improved the LabVIEW control and monitoring software.

C. THESIS OBJECTIVE

The previous section highlights the enormous amount of effort that has been put into the development of the DDAR concept by NPS students. Solutions to several key challenges have been proposed for a large part of the problem space. This research is a continuation of the effort to refine the design and performance of the demonstration array.

1. Main Objective

This thesis is addressing problems in the Systems Engineering (SE) domain as well as the more specialized Electrical Engineering (EE) domain. A main objective of this thesis is to:

Consolidate everything in a working two-module engineering model, up to and including synchronization and demonstration of transmission-reception between them. Furthermore, develop a Control and processing program that will handle all the functions that the module performs up to this milestone.

In order to fulfill this task, a series of tasks are to be performed. First, a large part of the previous work has to be verified and validated (V&V). An example is the verification of the demodulator board configuration. Furthermore, proof of concept must be performed for redesigned and redeveloped subsystems and components that were not working to the desired level. In that domain, the synchronization circuit is the main candidate. Finally, design and development of new components have to be done from scratch. Within this category, software components that handle the synchronization of the modules are to be designed and developed.

2. Design Principles

The design principles that will be followed in our work are presented below so the reader can follow the logic that led us to particular design solutions.

a. Hardware and Software Development

This thesis is an excellent opportunity to design and develop both hardware and software. Stable operating conditions of the hardware will be determined and then control and processing software will be developed. The reverse will also be true. Development of hardware and software at the same time will be avoided.

b. Modularity

The solution will be as modular as possible in order to allow future software and hardware modifications to expand the functionality of the radar without the need for a complete redesign. Burgstaller described a design for an array with eight modules. Although the eight-module design will not be attempted in our work, the module design will continue with this goal in mind.

c. Simplicity

The hardware and software solutions will be kept as simple as possible, since this is a proof of concept and not a fully functional system at this stage of the project. Furthermore, the components that are used are COTS and are of limited capability. The operating frequency, 2.4 GHz, is different than the actual frequency of the full scale radar (most likely HF or VHF). The availability of COTS hardware and the fact that no license is needed for operating in the 2.4 GHz and 5 GHz bands is the reason for this frequency selection.

d. Documentation

Documentation of all the work is of paramount importance in our project. The design and the test of the benchtop model will be documented as much as possible to serve as a reference.

D. THESIS ORGANIZATION

Chapter II briefly discusses the architecture of the DDAR system. Both the hardware architecture and the software architecture are addressed in this chapter. A short introduction is presented for all the top level components of the system.

Chapter III includes a review and verification of previous work. In addition, scattering parameters of all the equipment that is used for the construction of the new engineering models is presented.

Chapter IV addresses the main problem space. All the design and development work is included in this chapter. There is a description of the building process of the hardware. Furthermore, the software components such as the synchronization process and the waveform generator are presented in detail.

Chapter V demonstrates the new T/R modules and the LabView Software ("DDAR.lvproj"). A verification of the design is performed and the measurements are presented and discussed. In order to further investigate the results, simulations were run.

Finally Chapter VI presents the lessons that we learned from this project and our conclusions. There are also some insights and suggestions for future work.

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II. DESCRIPTION OF THE DDAR SYSTEM

A. ARCHITECTURE

1. Overview

The DDAR will be an integrated part of the ship. The array elements will be embedded in the ship's hull and need to be implemented during the early ship's design phase as shown in Figure 5. There will also be a centralized Controller for the management and operation of the system. The communication within the system will be done entirely by wireless technology. Two different wireless channels will be used. One channel will be used for the Local Oscillator (LO) distribution to synchronize the modules to a common reference. The other channel will be used for transmitting control signals and radar data.

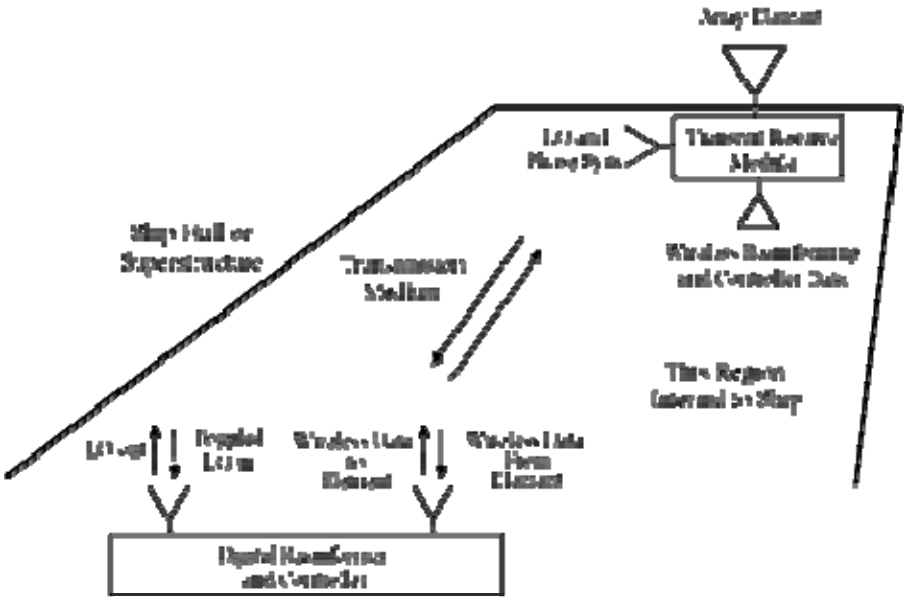


Figure 5. Architectural overview of the DDAR system (From [14])

The wireless channel is the internal space of the ship. Methods of improving the ship propagation environment are currently being developed. They include such things as

through bulkhead relays and integrated transmission systems. Figure 6 illustrates an integrated transmission system that would allow modules to be directly connected in order to transmit and receive data and synchronization signals.

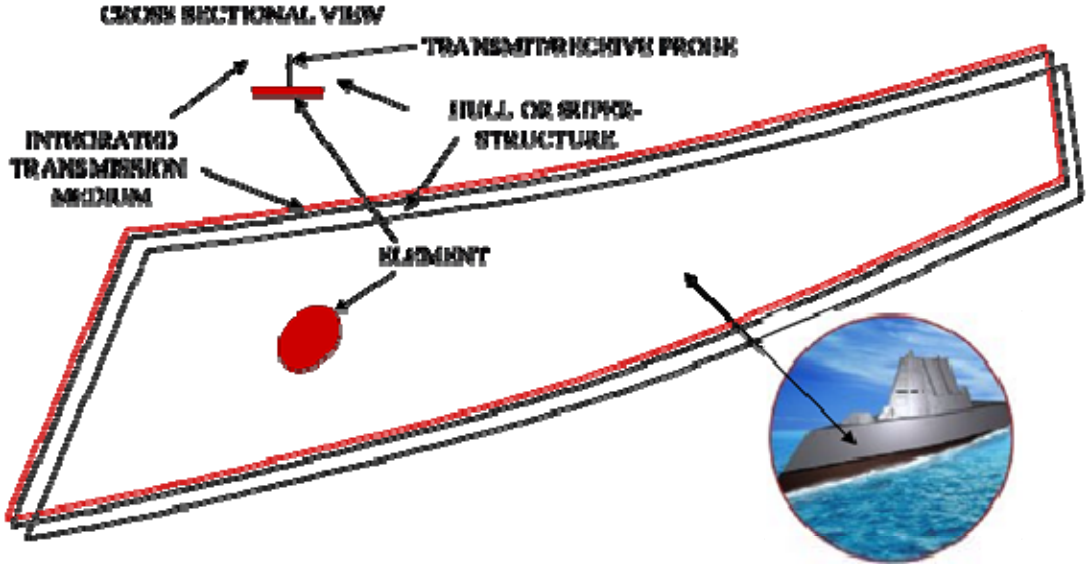


Figure 6. Integrated transmission medium (from [5])

One benefit of a wireless solution is a lighter structure, by avoiding the wires and transmission lines that would otherwise run all over the ship. Furthermore, the system does not impose any restrictions on the design of the hull and deckhouse because there is no dedicated large central space for the antenna. It is not necessary to cut out large areas of the ship surface to insert the antenna, which would weaken the structure. Battle damage will not disable the entire system but only the local parts affected by the attack. In addition, the T/R modules will be as small as possible and interchangeable, providing higher maintainability.

2. T/R Modules

The T/R modules are one of the most important parts of the system. Burgstaller and Yeo initially built the first two T/R modules. Grahn later modified them to include the synchronization circuit. Their current hardware configuration will be described in Chapter IV.

The function of the T/R module is to transmit the assigned signal and receive target returns and send the sampled returns back to the Controller. A simplified version of the T/R module is shown in Figure 7. The sequence of events is as follows. Once deployed, the T/R module must synchronize its phase to a reference. Next, when in transmit mode, the Controller sends a control and waveform information to the T/R module's local controller via the wireless network. The baseband waveform is generated at each element, up converted, and then transmission of the waveform occurs simultaneously from all elements. When operating in receive mode, the incoming radar echo is amplified by a Low Noise Amplifier (LNA) and then it is directed to the demodulator board. There, the signal is mixed with the LO signal and the resulting baseband signal is sampled and sent back to the Controller via the wireless network. The radar processing and beamforming are done in the Controller.

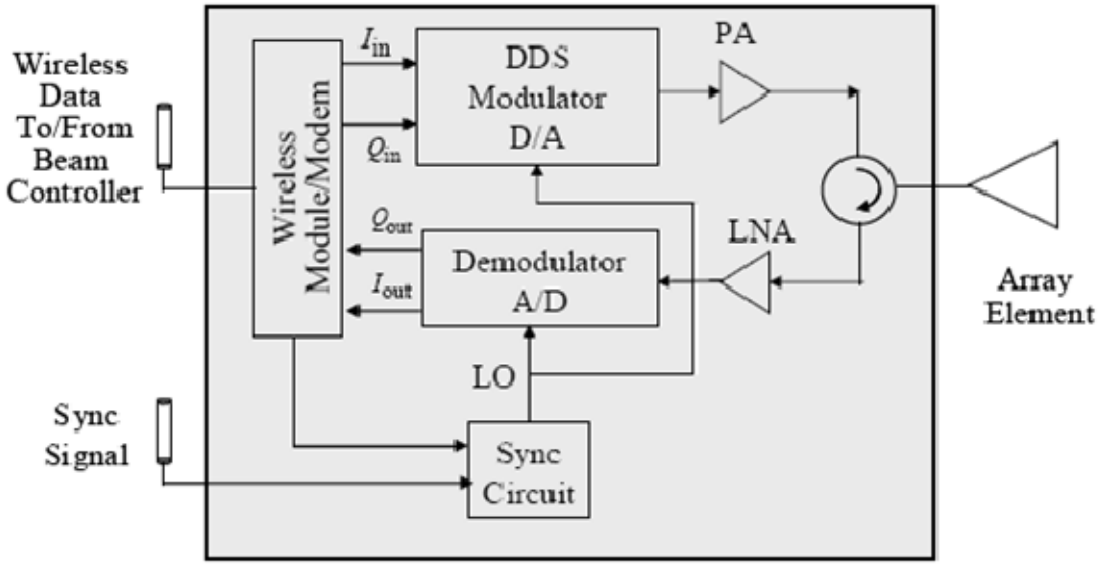


Figure 7. Operating concept of the T/R module (from [7])

3. Controller

The heart of the DDAR system is the master controller and digital beamformer (simply referred to as the Controller). It is the central computer that is responsible for the operation of the system. It distributes the desired control signals to the T/R modules and synthesizes their responses to extract the requested information by the operator. The Controller generates the beamforming as well as all the waveform parameters and supervises all communications and data transfer between the modules. A LabVIEW application running on the Controller is used to perform these tasks. The demonstration array has limited capability, so not all radar tasks are performed by the Controller. The functions of the Controller for the demonstration module are depicted in Figure 8.

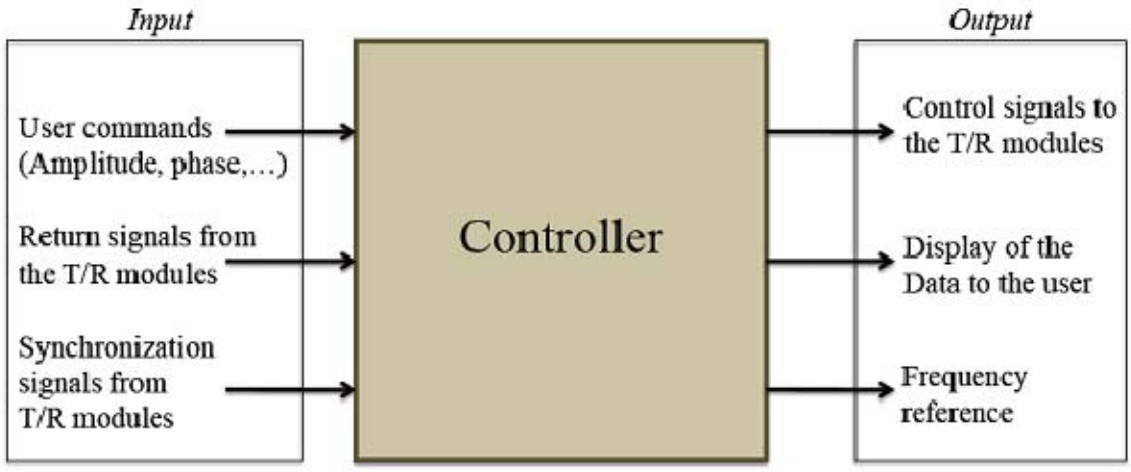


Figure 8. The Controller functions

4. LabVIEW

The development of the DDAR requires a programming suite that can create a Graphical User Interface (GUI), can be used for field programmable gate array (FPGA) programming, have compatibility with the hardware, and can allow the design of network applications that share data. Furthermore, it should be capable of rapid application development (RAD). For the above reasons LabVIEW was chosen.

The applications developed are for both the Controller computer and the individual T/R module FPGAs. The software was initially written by Yeo, and subsequently modified by Noris. The current version of the main function GUI is shown in Figure 9. The various functions are described in Chapter IV and Appendix A.

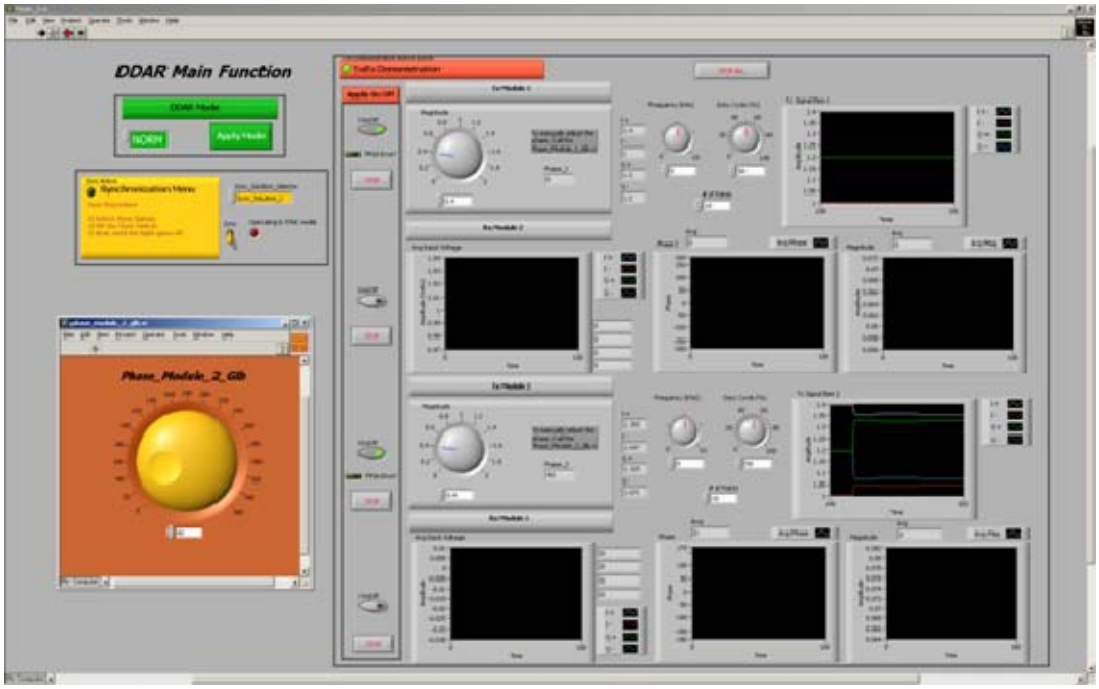


Figure 9. Main Controller GUI

5. Wireless Network

The wireless network that is used for the communication between the Controller and the T/R Modules is the IEEE 802.11a. It is operating at 5 GHz so it does not interfere with the LO-system that operates at 2.4 GHz. In the two element array, the network is implemented by the use of a wireless access point (WAP) attached to the controller computer. One wireless bridge per module connects it to the WAP. For a more detailed description of the wireless network the reader is referred to the thesis by Noris [13].

6. LO-system

The LO-system operates at 2.4 GHz. The purpose of the LO-signal is two fold. One of the functions is to provide a reference for synchronization of the T/R modules. The phase of the LO-signal on one of the modules is used as a reference to which all the other modules in the system are synchronized. The phase difference of the LO-signal between the reference and each of the other modules is the information obtained in the synchronization process. The measured phase difference is corrected for in digital processing. The second function of the LO-system is to provide the carrier frequency of the radar to the modulators and demodulators. The beacon itself serves as the LO signal for all modules.

B. HARDWARE COMPONENTS

This section provides a summary of the equipment that is used within the scope of the DDAR project. Table 1 gives the critical components along with the relevant thesis sections and references. Also refer to Chapter III for the scattering parameters of each component.

Component	Model	Remark
WAP	D-Link DWL-7100AP	Page 46 in [9], and D-Link manual [15]
Wireless bridge	3COM WL-560	Page 47 in [9], and 3COM manual [16]
Real time controller	NI cRIO-9004	Page 43 in [8], page 34 [10], and National instruments [17]
FPGA	NI cRIO-9101 and NI cRIO-9103	Page 43 in [8], page 35 in [10], and National Instruments [18]
Digital to analog converter (DAC)	NI cRIO-9263	Page 43 in [8], page 36 in [10], and National Instruments [19]
Analog to digital converter (ADC)	NI cRIO-9215	Page 43 in [8], page 36 in [10], and National Instruments [20]
Transistor transistor logic (TTL)	NI cRIO-9401	Page 49 in [9], and National Instruments [21]
Modulator board	Analog Devices AD8346	Page 29 in [7], and Analog Devices [22]
Demodulator board	Analog Devices AD8347	Page 59 in [7], and Analog Devices [23]
Low power amplifier (LPA)	RF Bay LPA-4-14	Page 38 in [7] and, RF Bay [24]
Low noise amplifier (LNA)	RF Bay LNA-2700	Page 53 in [7] and, RF Bay [25]
Switch	Mini-Circuits ZASWA-2-50DR	Page 38 in [9] and, Mini-Circuits [26]
Splitter	Pasternack PE2014	Pasternack [27]

Table 1. Components references

C. SUMMARY

In this chapter, the architecture of the DDAR system was presented. All the high-level components are identified. They include the T/R modules, Controller, LabVIEW software, wireless network components, and the LO-system. Furthermore, their purpose and the interactions among them were made clear. The components of the system are

listed alongside with the corresponding references. Both the hardware design and datasheets of the manufacturers, as well as the research performed by the previous students are pointed out.

The next chapter discusses the synchronization problem within the existing T/R modules. It also describes the verification of previous work regarding the demodulator board; the investigation of automatic gain control (AGC) versus a fixed gain (VGIN). Finally, Chapter III includes the scattering parameters for the components used in the two new T/R modules.

III. VERIFICATION OF PREVIOUS WORK AND HARDWARE PERFORMANCE

A. BACKGROUND

In order to continue with the DDAR project, a few preliminary steps were needed to acquire the most accurate information as to where changes and new implementations are to be done. The weaknesses in the design that surfaced in previous theses seemed to have their roots deeper in the early days of the project. For that reason this chapter describes the identification of the problems and re-evaluation and verification of the previous work. The first item addressed is the existing design of the synchronization circuit. The present technique for synchronization is one of many possible methods. It was selected because of its simple hardware implementation. The circuit seemed to be performing well in wired mode, but lacked the same capability in wireless mode. The second problem that surfaced during the investigation of possible new candidates for the demodulator board was the small dynamic range of the AD8347 due to the use of a constant voltage gain (VGIN). In this work the Automatic Gain Control (AGC) function of the board is re-evaluated. The last part of this chapter presents the up-to-date performance of all the hardware components that are used in the new T/R modules. This provides a knowledge base for the expected overall module performance.

B. SYNCHRONIZATION CIRCUIT

Grahn recognized a potential problem in the synchronization circuit during the measurement of "setup E" in his thesis [12]. In this setup the LPA is located in the synchronization circuit to improve the maximum distance that the T/R modules could be set apart and still be able to be synchronized wirelessly. Secondary signals from reflection and leakage appeared to be filling and shifting the destructive notches that are used to estimate the synchronization phase.

An attempt to replicate the results that were acquired by Grahn was conducted in order to investigate the problem. Repeating the measurement in "setup C" in [12] for

verification was suggested. In this set up, an attempt to synchronize the two T/R modules through the use of a hardwired LO-distribution was performed. The block diagram of "setup C" is replicated in Figure 10.

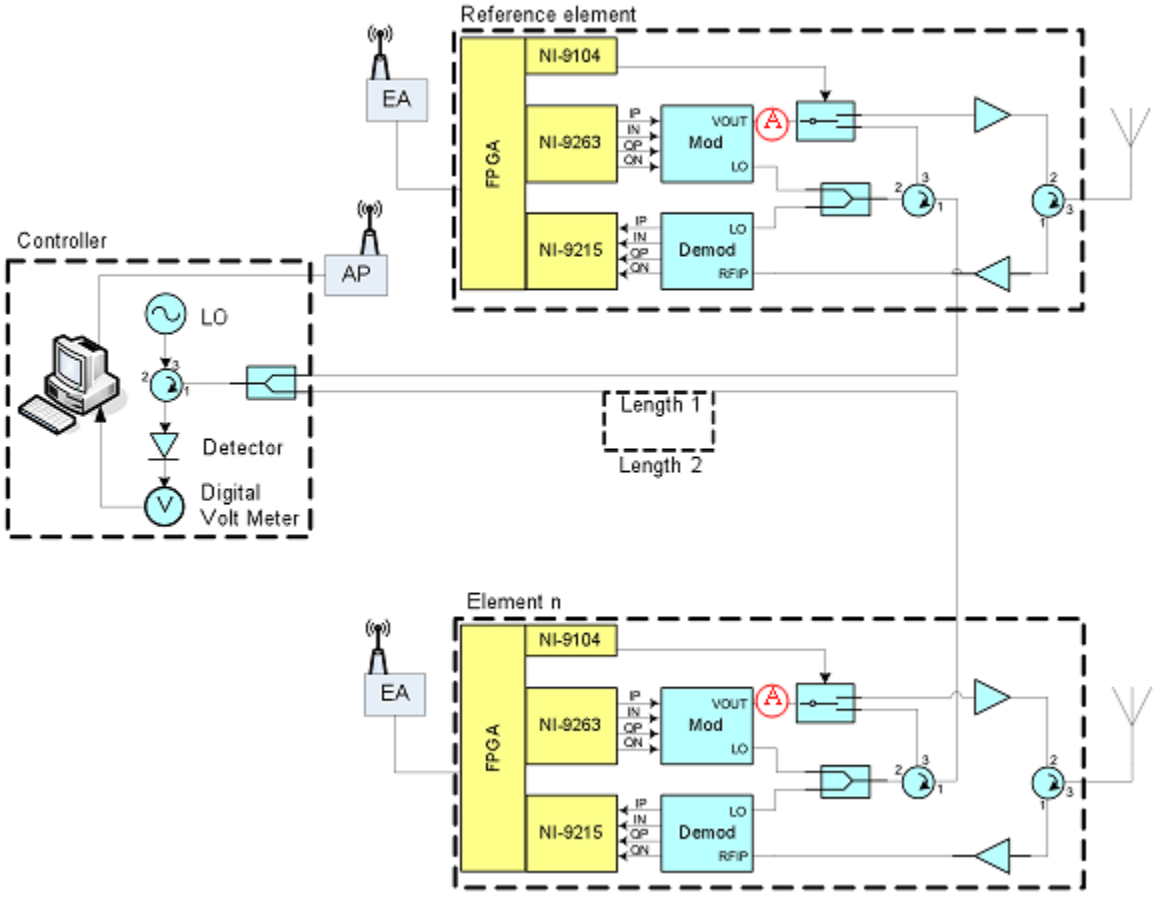


Figure 10. "Setup C" (From [12])

It should be stressed that in "setup C", the LPA is not inside the synchronization circuit. In order to verify the synchronization, the expected phase difference between cable paths ("Length-1" and "Length-2") is calculated before the experiment begins. The conversion of the one-way physical path difference to the phase difference can be derived by

$$\varphi = \frac{d}{\lambda} \times 360° \tag{1}$$

where φ is the phase difference between the two cables in degrees, d is the physical length difference between the cables in meters, and λ is the wavelength in the cable in meters[2].

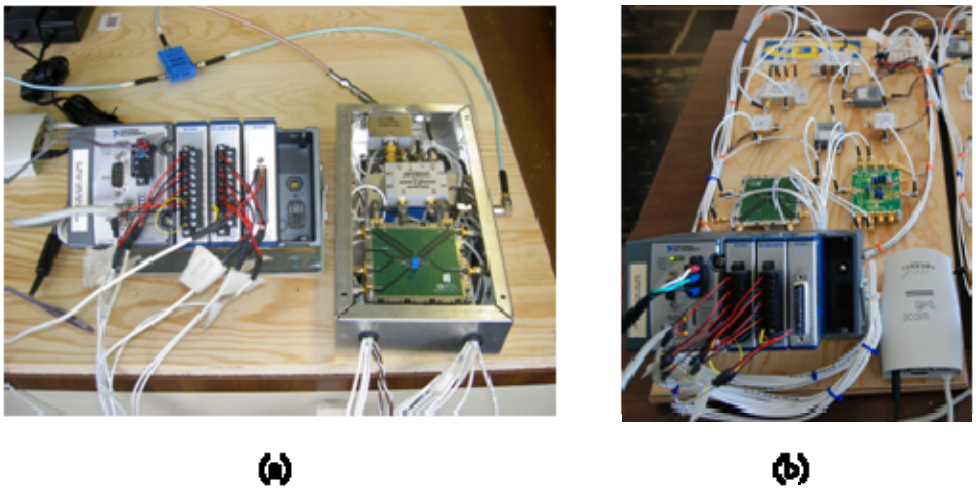
The procedure to measure the phase difference is to attach the cable with "Length-1" to the setup, and then find the minimum amplitude on the voltmeter, as the phase of the module under synchronization is incremented through a 360 degree cycle. Next, replace the "Length-1" cable with the "Length-2" one and repeat the measurements. Direct comparison of the two acquired curves and their minimum values will yield the measured phase difference. Note that measured phase difference should be twice the value given by (1). The reference LO is shifted by φ on its path to the modulator, and the transmitted RF is shifted again by φ on the return path.

The physical path difference of 14 mm used in Grahn's thesis is expected to produce a one-way phase difference of 40.3 degrees between the two T/R modules. This result was approximately acquired experimentally in [12] by getting a measured phase difference of 50 degrees by following the procedure described in the previous paragraph.

The test points for verification in the T/R modules were un-accessible in the assembled RF portion of the T/R modules. It was deemed to be considerably difficult to disassemble them, thus making it impractical to move the LPA out of the synchronization circuit. In order to facilitate measurements, a new pair of T/R modules were designed and built in a more modular way that allows easy reconfiguration of the components. The

[2] The cable used is RG-316 which has a phase velocity 70% of the speed of light, i.e., 2.06 x 10^8 m/s.

design and implementation of the modules is described in Chapter IV and their behavior is demonstrated in Chapter V. The accessibility of test points is evident by comparing the photos in Figure 11.



(a) (b)

Figure 11. Photos of the two T/R module layouts. (a) Boxed RF system and (b) benchtop configuration

"Setup C" was tested on the existing T/R modules used by Grahn, where the LPA is located at point "A" in Figure 10. The measured data is shown in Figure 12. The results appear to be affected by the increased power level from the LPA that is mounted in the synchronization circuit.

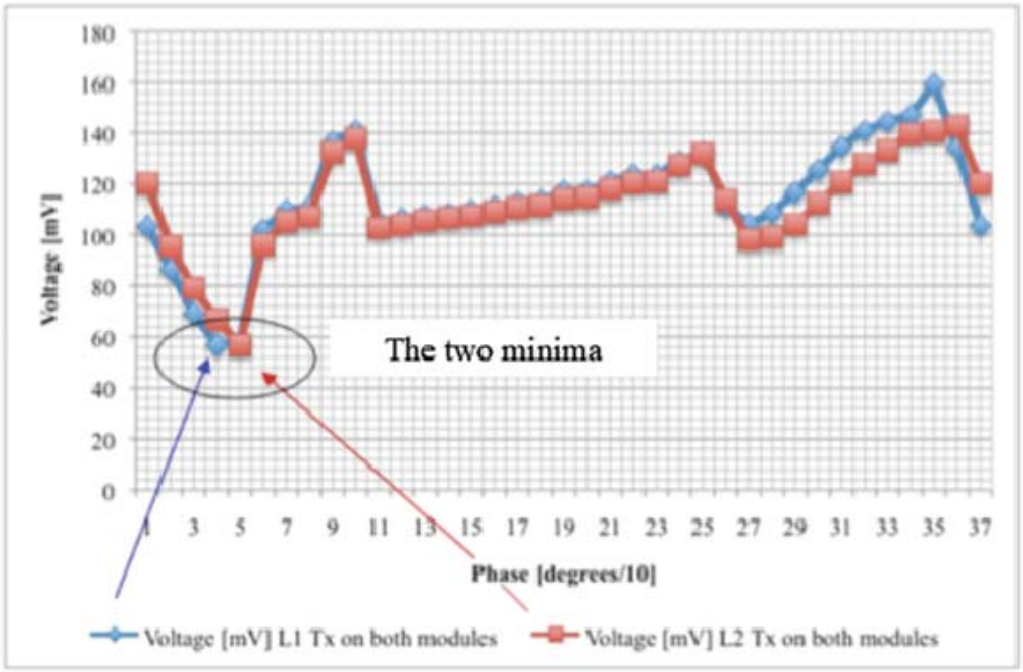


Figure 12. Phase comparison between the two cables with LPA

The two cables ("Length-1" and "Length-2") that were used in this experiment had a physical length difference of 24 mm. The expected one-way phase difference was calculated to be 100.6 degrees. As it can be seen from Figure 12, the measured phase difference (difference in minima locations) is approximately 10 degrees two-way or 5 degrees for one-way propagation.

The result indicates that after the LPA was included in the synchronization circuit, the phase information was distorted due to power returning through the circulator. (The curves should have a sinusoidal shape vs. phase.) Therefore, the circuit was redesigned and implemented in the new T/R modules. The new circuit is described in detail in Chapter IV.

C. DEMODULATOR BOARD

1. Background

In order to evaluate and verify previous conclusions about the behavior of the demodulator board, measurements were repeated on boards numbered #14, #15, and #12. The measurements and their results are found in several previous thesis reports, but most of the measurements were performed to specific responses, such as the linearity of response for a fixed value of RFIN. The following section describes the procedure of how to perform the phase measurement and also contains the results from new measurements, including different RF input levels.

2. Experimental Setup

Measurement and evaluation of the linearity and the dynamic range for the AD8347 demodulator board was done with two different setups. The first two boards were measured in the AGC mode (demodulator boards #14 and #15). In order to verify the VGIN mode, a complete phase measurement over 360 degrees was performed on demodulator board #12. The exterior setup for the two different cases (AGC or VGIN) just differs in the connection of pin #17 (VGIN) that is used in the VGIN mode. The following six step procedure should be performed to measure the in-phase and quadrature-phase responses (I- and Q-responses) from the demodulator boards.

a. Step 1

Attach the demodulator board to the test rig, as shown in Figure 13 using four screws to fix its position. Connect RFIN, LOIN, IPP, IPN, QPP, QPN, and 5V to the board as in Figure 14. (Do this for the AGC MODE; if VGIN mode is to be measured connect desired voltage level to connection #17, e.g. 0.38V.)

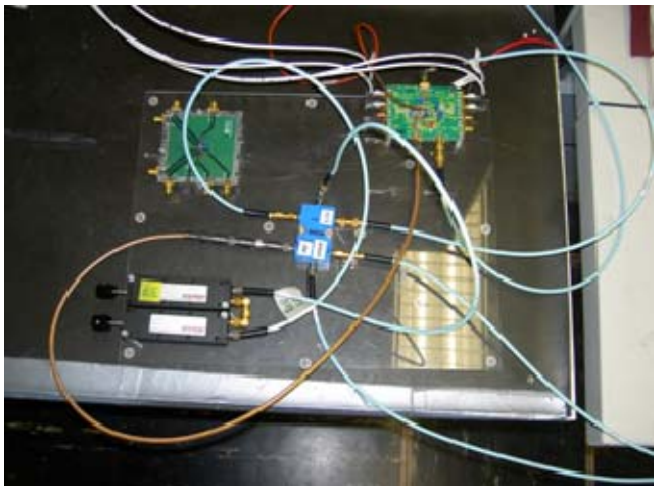


Figure 13. Test rig for demodulator measurements

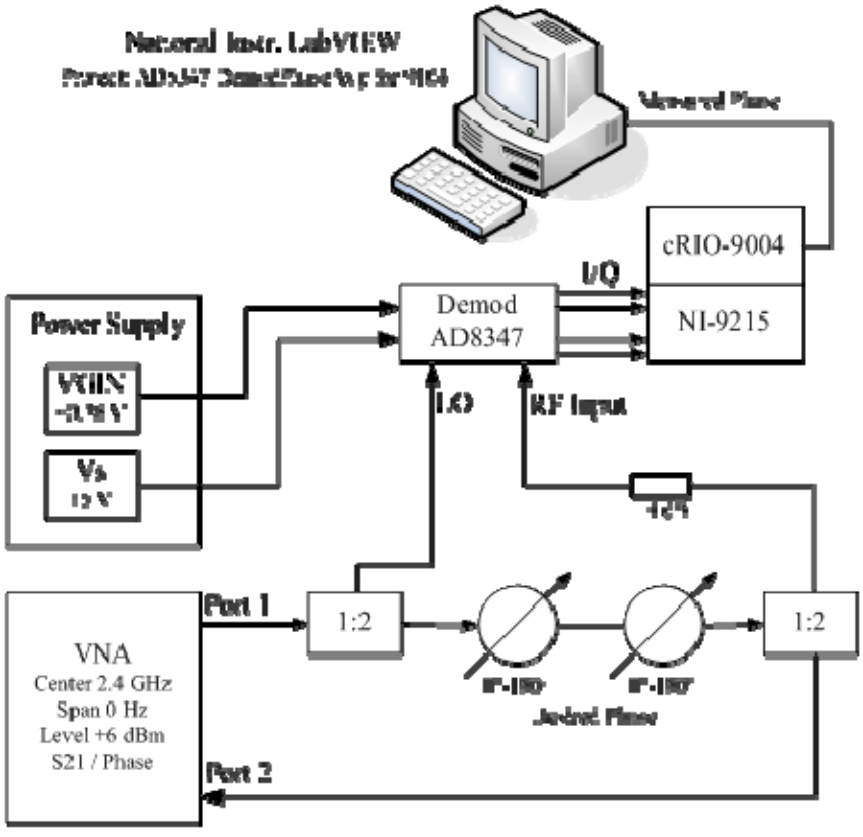


Figure 14. AD8347 Demodulator phase calibration setup (From [12])

b. Step 2

The LO and RF signals will be provided by the VNA HP8510C [28]. The control panels of the VNA are shown in Figure 15 and the settings for the measurements are found in Table 2. Due to the fact that the measurement is over a fixed frequency (2.4 GHz), the VNA does not need to be calibrated. Port 1 is used for the LO and RF output power to the test rig and port 2 is used to measure the phase shift added by the phase shifters (see step 3).

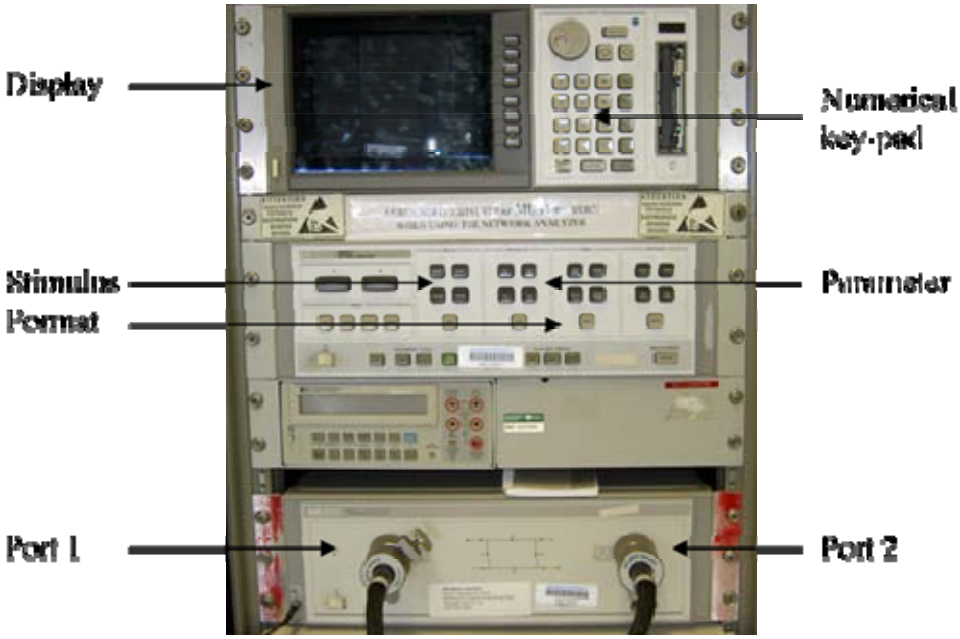


Figure 15. VNA control panels

Parameter	Setting/Value	Press
Operating frequency	2.4 GHz CW	STIMULUS CENTER 2 . 4 G/n
Span	0 Hz	STIMULUS SPAN 0 x1
Power level	+6 dBm	STIMULUS MENU Port 1 6 x1
Type of measurement	Phase	FORMAT PHASE
S-Parameter	S_{21}	PARAMETER S_{21}
Sweep rate	51	STIMULUS MENU number of points 51
Set start-phase to zero	0	DISPLAY Data to mem 2 Math (./)

Table 2. VNA settings for calibrating the demodulator

c. Step 3

The phase shift in the setup is introduced with two Sage phase shifters (see Figure 16). Each of them can shift the phase up to 180 degrees. With two connected in series the phase input to the demodulator can be adjusted from 0 to 360 degrees. The phase shifters have a frequency range of DC – 8 GHz and an insertion loss of 0.7 dB. When starting the measurement the phase shifters should be turned to their endpoints. (Do this by turning the knob counter clockwise until it stops.)

Figure 16. Sage phase shifters

d. Step 4

Next, for ease of reading the phase, set the scale on the VNA display to 45 degrees/division and the reference level to zero.

e. Step 5

The voltage levels on IPP, IPN, QPP, and QPN are connected to the NI-9215 analog-to-digital module, which is connected to the computer running LabVIEW. To read the values from the in-phase and quadrature-phase channels the project “AD8347 DemodPhaseAvg for 9104.vi” is used. To start the program start LabVIEW and run the “AD8347 DemodPhaseAvg for 9104.vi” project. To choose the target FPGA-module you scroll down to “VISA Resource-menu” and find the address “visa://169.254.0.2/RIO0::INSTR.” This can take some time due to the handshake procedures that take place between the host and FPGA. Before you run the program be sure to reset the MATLAB script for the I and Q values to correct the DC offset of the

board under test. Also, select the measurement file of your choice. To start the measurements just press the run arrow in the top left toolbar. The average voltage values are taken every time the button “STORE” is pressed (see Figure 17). These values are saved in a spreadsheet (rename the file otherwise the old file will be overwritten).

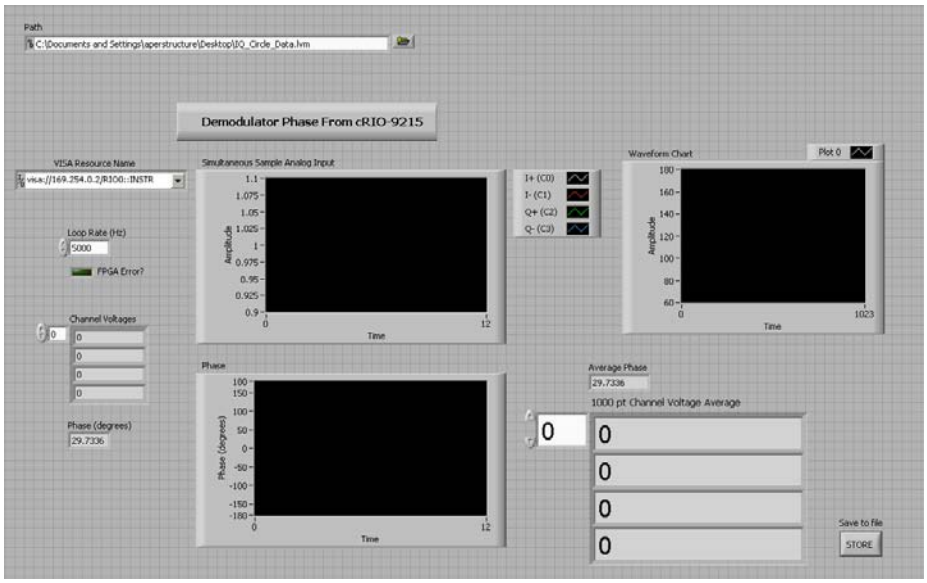


Figure 17. AD8347 DemodPhaseAvg for 9104.vi

To get enough resolution, the phase should not be shifted in more than 30 degree steps to be able to plot the I/Q circle accurately. After shifting the phase, wait 30-40 seconds for the values to stabilize before pressing the “STORE” button. Continue taking samples until coverage of 360 degrees have been achieved.

f. Step 6

The last step is to extract the sampled data in MATLAB to get a plot of the I/Q circle. An example of the MATLAB program used for one of the measurements is presented in Figure 18. This script was originally written by Burgstaller and modified for each measurement.

```
% Phase Mesuremenents, 03.04.2008
% Demodulatorboard #14 with LO power -10dBm, AGC function

% A --> Magnitude
% P --> Phase
% X --> M*cos(P)
% Y --> M*sin(P)

clc;clear;

%A = xlsread('Phase_Measurements_VGIN_0_3V', 'I2:I59');
%P = xlsread('Phase_Measurements_VGIN_0_3V','J2:J59');
%X = xlsread('Phase_Measurements_VGIN_0_3V','K2:K59');
%Y = xlsread('Phase_Measurements_VGIN_0_3V','L2:L59');

I = xlsread('Phase_Measure_AGC_LOneg10dbm_RFneg12_Board_14','G2:G13');
Q = xlsread('Phase_Measure_AGC_LOneg10dbm_RFneg12_Board_14','H2:H13');

i=mean(I);
q=mean(Q);

dI=max(I)-min(I);
dQ=max(Q)-min(Q);

figure(1)
plot(I-mean(I),Q-mean(Q),'r-',I,Q,'b*',i,q,'g+');
grid on;
title(['Board 14 (AGC) (LOin -10dBm) (RFin -12dBm),( \DeltaI = ', ...
    num2str(dI),' \DeltaQ =' ,num2str(dQ), ' Offcenter = I :', ...
    num2str(i),', Q :' ,num2str(q),' )']);
xlabel('I'); ylabel('Q'); axis equal;
```

Figure 18. MATLAB program for plotting the I/Q circle

3. Measurements and Results

The performance of board #14 was measured with a LO input of both -10 dBm and -11 dBm at the frequency 2.4 GHz. The RF input signal level (RFIN) was shifted from -61 dBm up to -12 dBm. The board was configured and measured in the AGC mode. The results for the different LO and RF levels can be seen in Figure 19 to Figure 27.

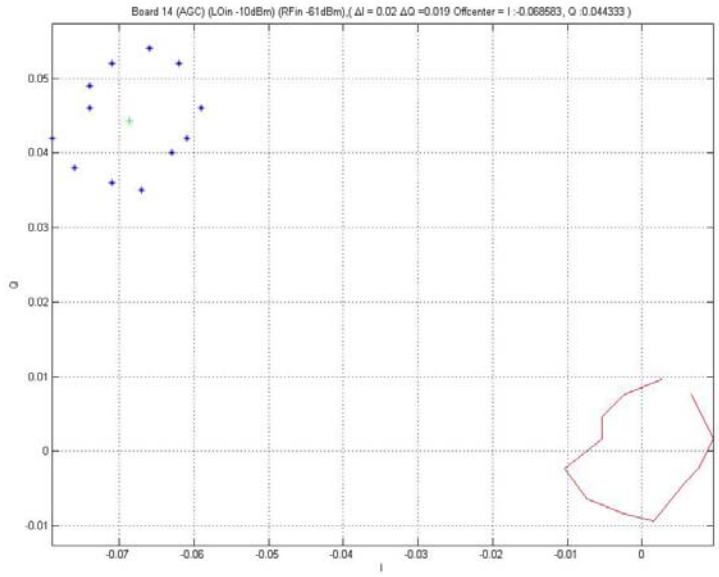


Figure 19. Board #14 (LO -10 dBm, RFIN -61 dBm, Circle radius ~0.01 V)

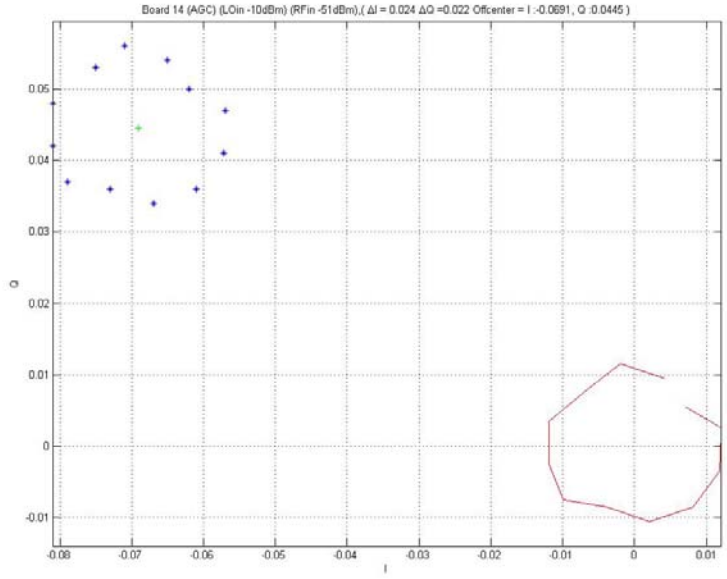


Figure 20. Board #14 (LO -10 dBm, RFIN -51 dBm, Circle radius ~0.012 V)

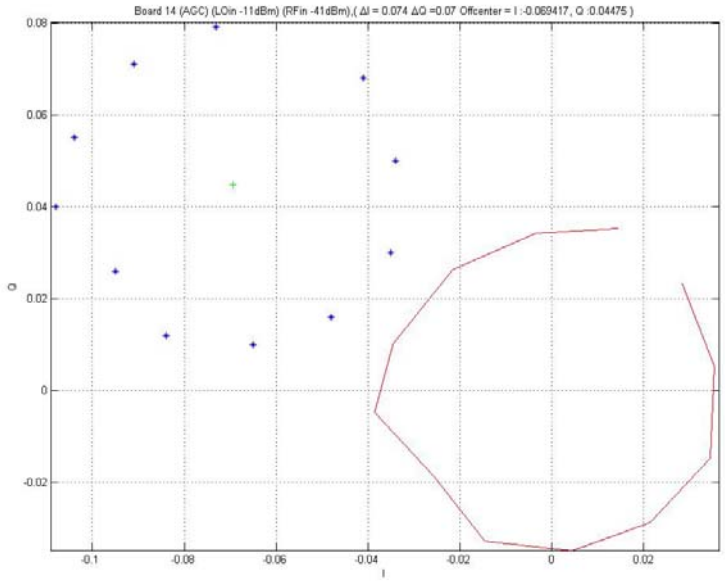


Figure 21. Board #14 (LO -11 dBm, RFIN -41 dBm, Circle radius ~0.035 V)

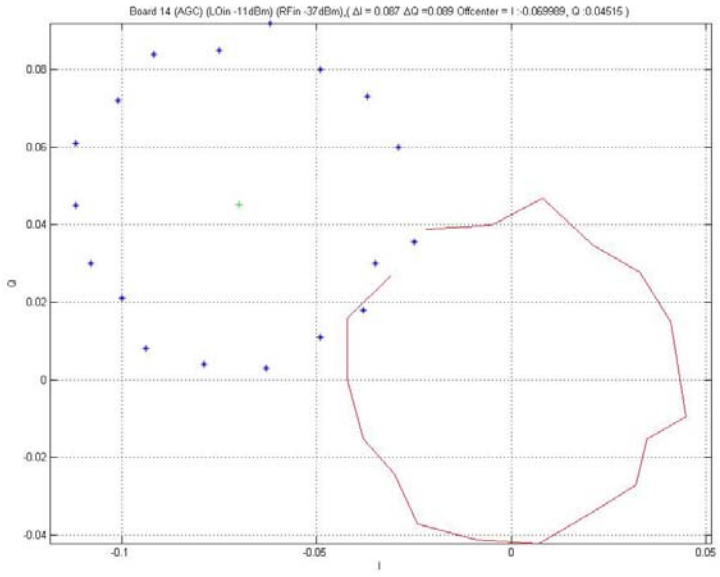


Figure 22. Board #14 (LO -11 dBm, RFIN -37 dBm, Circle radius ~0.042 V)

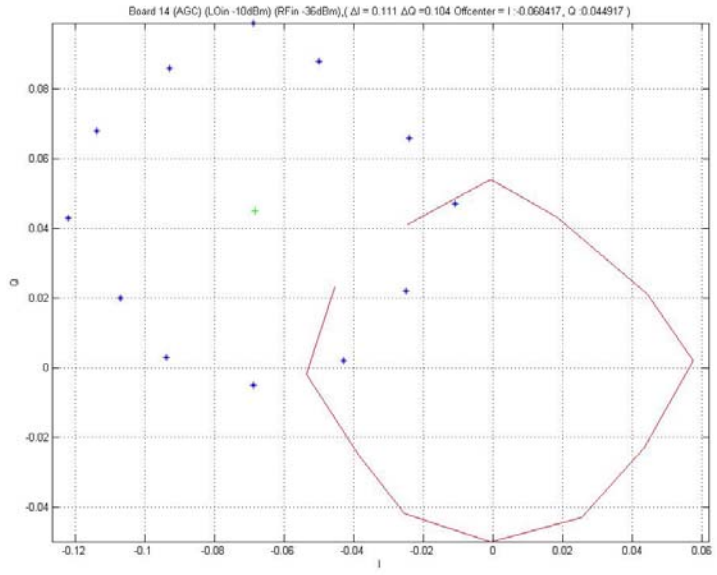


Figure 23. Board #14 (LO -10 dBm, RFIN -36 dBm, Circle radius ~0.051 V)

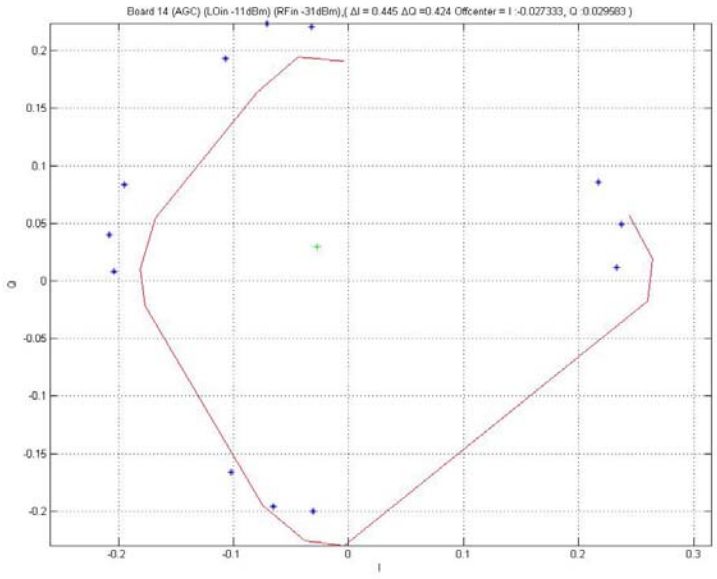


Figure 24. Board #14 (LO -11 dBm, RFIN -31dBm, Circle radius ~0.2 V)

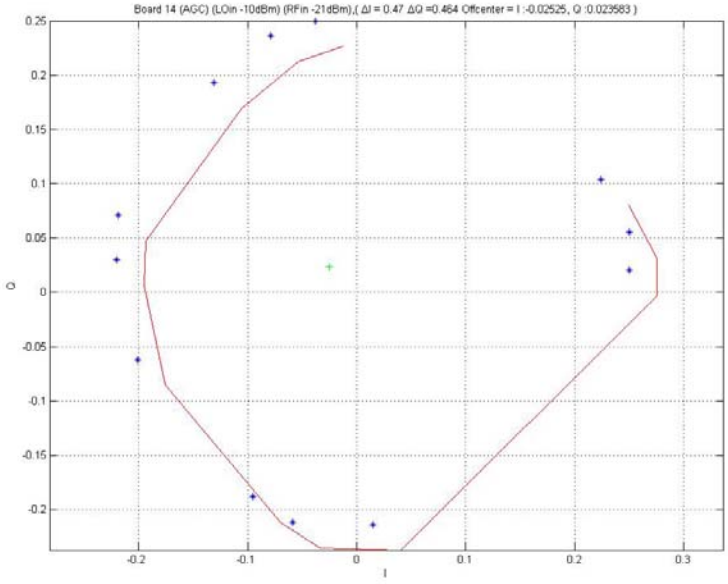


Figure 25. Board #14 (LO -10 dBm, RFIN -21 dBm, Circle radius ~0.24 V)

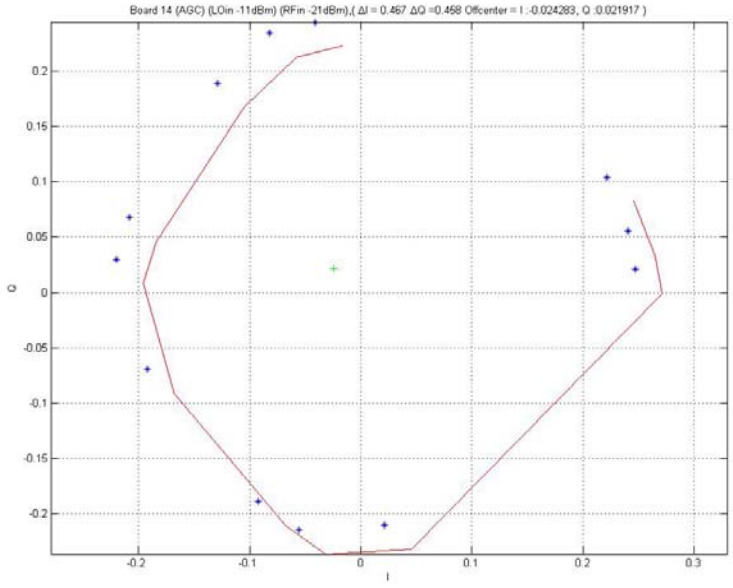


Figure 26. Board #14 (LO -11 dBm, RFIN -21 dBm, Circle radius ~0.25 V)

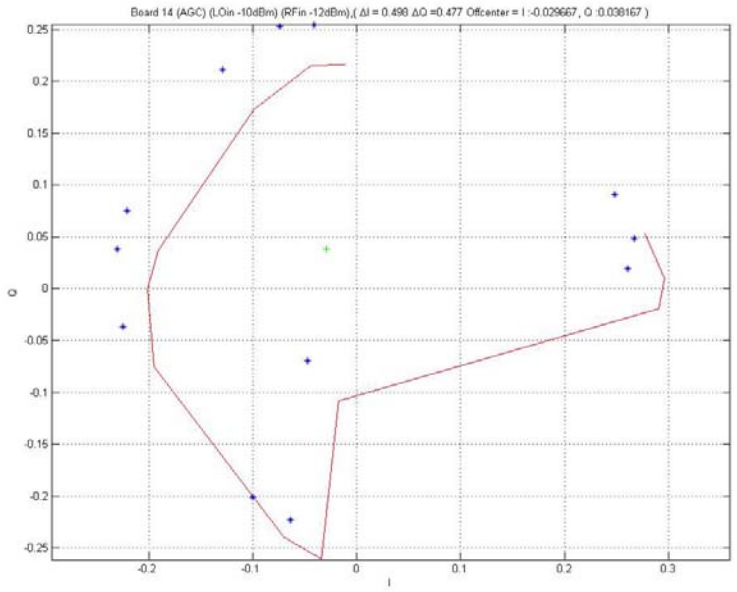


Figure 27. Board #14 (LO -10 dBm, RFIN -12 dBm, Circle radius ~0.025 V)

The same measurements were taken on board #15. The results for the different LO and RFIN values were almost identical to those of board #14.

The results shows that there is no significant difference between the LO input level of -10 dBm or -11 dBm. Measurements were also performed with a LO input level of -8 dBm (not included in the figures) and the performance of the demodulator board was not as stable as in the -10 dBm and -11 dBm cases. The I/Q-channel phase output shows a linear relation with the RF-input values between -61 dBm and -36 dBm. When the RF-input signal is stronger, in the range of -21 dBm up to -12 dBm, the phase values tend to be forced by the AGC towards the X and Y axis, instead of giving a circle around the origin. The figures also show that the radius of the circle is highly dependent on the RF-input level. The radius of the circle spans from 0.01V at -61 dBm RF-input up to 0.05V at -36 dBm RF-input, and continues to increase with increasing RF-input. However, above -21 dBm of RF-input the phase output is no longer linear.

To further investigate the linearity of the AGC function new measurements were performed. The reason for this was to look at the endpoints to find out the actual dynamic range for the demodulator boards. Table 3 shows the results for all measurements including the first AGC records.

Board	Function	LO in [dBm]	RF in [dBm]	Circle radius [V]	I offset [V]	Q offset [V]	Circle
14	AGC	-11	-33	0.062	-0.0665	0.0421	Almost
14	AGC	-10	-36	0.053	-0.0684	0.0449	Yes
14	AGC	-11	-37	0.05	-0.067	0.0451	Yes
14	AGC	-11	-41	0.032	-0.0694	0.0447	Yes
14	AGC	-10	-51	0.012	-0.0691	0.0445	Yes
14	AGC	-10	-61	0.01	-0.0686	0.0443	Yes
14	AGC	-11	-63	0.005	-0.0696	0.0444	Yes
15	AGC	-11	-33	0.075	-0.0157	0.0219	Almost
15	AGC	-10	-36	0.055	-0.0232	0.0287	Yes
15	AGC	-10	-40	0.028	-0.0217	0.0304	Yes
15	AGC	-10	-50	0.015	-0.0219	0.0303	Yes
15	AGC	-11	-54	0.011	-0.0212	0.0301	Yes
15	AGC	-11	-57	0.011	-0.0211	0.0301	Yes
15	AGC	-11	-60	0.01	-0.0209	0.0296	Yes

Table 3. Measurements result for board #14 and board #15

The results from the measurements show that it is possible to acquire linearity for RFIN values between -36 dBm down to -61 dBm. So while the demodulator board strapped to work in the AGC mode has a dynamic range of at least 25 dB, in the VGIN mode the practical dynamic range is just somewhere around 7 dB. As mentioned previously, the circle radius increases with increasing RFIN signal (see Figure 28). This can be corrected by varying the amplification of the RFIN signal. Furthermore, the offset values for the RFIN signal circles are almost the same over the entire dynamic range (see Figure 29 and Figure 30). This means that the offset that is calculated by the MATLAB script described in Chapter III in [10] and is used as a numeric constant in the "DDAR.lvproj" will work in the same way for the AGC mode as for the VGIN mode.

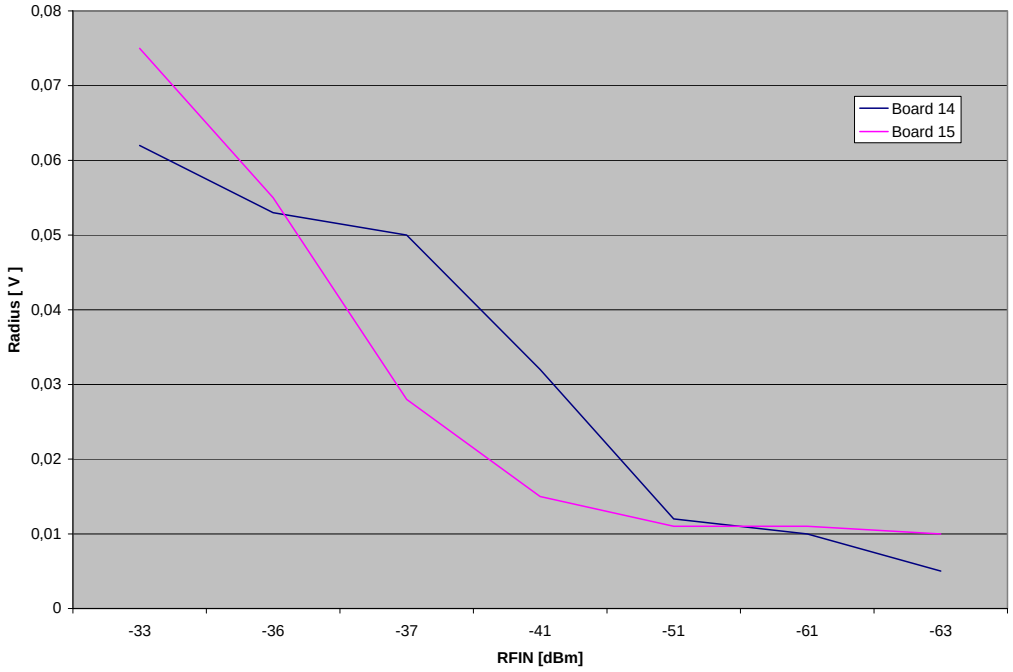


Figure 28. Circle radius for board #14 and board #15 vs. RF input power

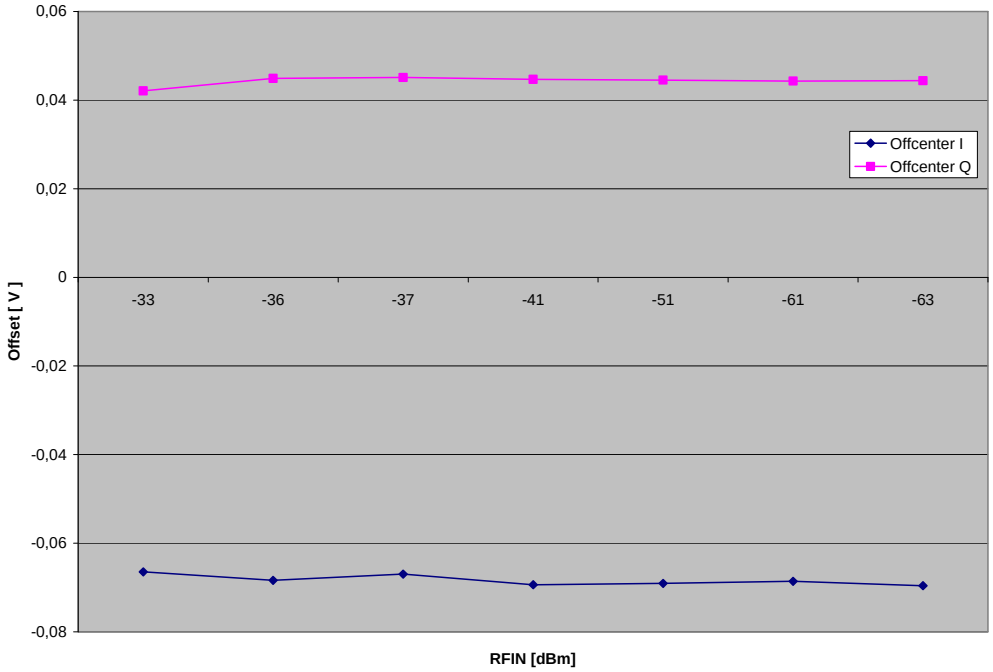


Figure 29. I and Q channel offsets for board #14

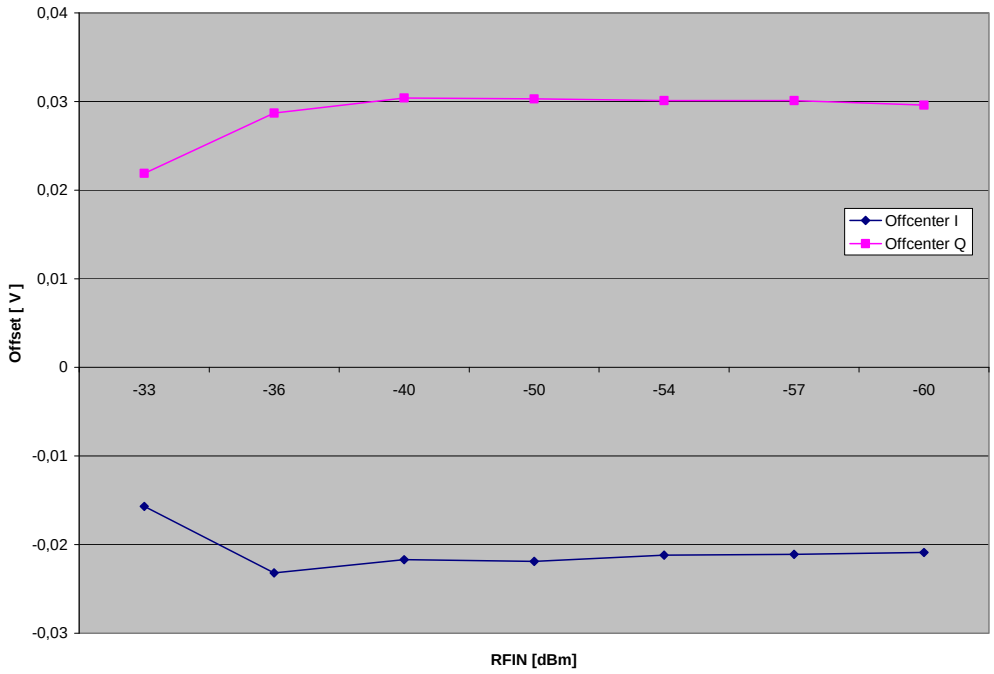


Figure 30. I and Q channel offsets for board #15

4. Summary

This section has analyzed the demodulator board's functionality in both VGIN- and AGC-modes. The new measurements that were performed gave the result that the demodulator board has a dynamic range of ~25 dB when strapped for operating in the AGC mode. (The AD8347 spec sheet [23] shows a linear range of approximately 65 dB but this is at 1.9 MHz.) If the RFIN signal strength is adjusted it is possible to achieve a relatively constant I-Q circle radius. The offset correction needs to be measured only once for each demodulator board, due to the nearly constant value over the entire measured RF input range.

D. SCATTERING PARAMETERS

1. Background

To compare the vendors' specifications of the components for the new T/R modules, scattering parameters were measured. All the components that were evaluated met the specifications. The following section briefly describes the components and shows a summary of the results of the measurements performed. For a detailed presentation of the entire measurements see Appendix B. The VNA HP8510C [28] was used for the scattering parameter measurements (see Figure 31).

Figure 31. VNA HP8510C

2. Splitter

The splitters used for the new T/R modules are from Pasternack Enterprises, and one is shown in Figure 32.

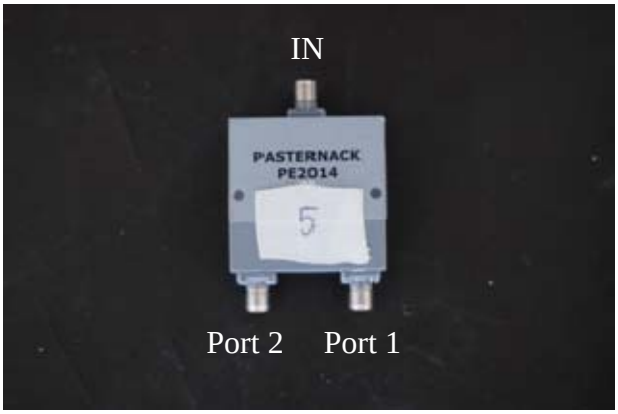


Figure 32. Splitter Pasternack PE2014

Four splitters are used, but measurements were done for five splitters. They are labeled from 1 to 5 and they will be referred accordingly. The port not connected to the VNA was terminated in a matched load. The results for the splitters are presented in Table 4. All splitters met the specifications which are given in Table 5.

	Splitter_1		**Splitter_2**		**Splitter_3**		Unit
	IN-Port1	IN-Port2	IN-Port1	IN-Port2	IN-Port1	IN-Port2	
S11	1.1183	1.1168	1.142	1.1414	1.1371	1.1418	SWR
S12	-3.4198	-3.2698	-3.3477	-3.347	-3.3682	-3.3038	dB
S21	-3.2666	-3.1201	-3.1967	-3.1951	-3.2158	-3.1509	dB
S22	1.0999	1.0413	1.0315	1.0132	1.0143	1.024	SWR

	Splitter_4		**Splitter_5**		Unit
	IN-Port1	IN-Port2	IN-Port1	IN-Port2	
S11	1.1622	1.1606	1.1415	1.1395	SWR
S12	-3.302	-3.394	-3.3208	-3.3872	dB
S21	-3.147	-3.1924	-3.1687	-3.2356	dB
S22	1.0156	1.0129	1.0352	1.037	SWR

Table 4. Measured scattering parameters for Splitters 1-5

Specification	Value	Unit
Freq. Range	2-4	GHz
Max. VSWR	1.3	SWR
Max. ins. Loss	0.3	dB

Table 5. Vendors' specification for the splitter

3. Switch

Zaswa-2-50DR are the switches of choice (see Figure 33). The switch is a high isolation wideband component. Measurements were performed on 4 switches and the results are shown in Table 6. Each switch was measured over the two output ports and the isolation was measured when the actual port connected was closed. The output port not connected to the VNA was terminated in a matched load.

Figure 33. Switch ZASWA-2-50DR

	Switch 3		Switch 5		Unit
	IN-Port1	IN-Port2	IN-Port1	IN-Port2	
S11	1.6523		1.6639		SWR
S12	-2.0601	-1.982	-2.0983	-2.0061	dB
S21	-1.934	-1.8392	-1.9528	-1.8578	dB
S22	1.2826	1.1895	1.2646	1.1898	SWR
S12 with switch Off	-75.91	-80.359	-73.871	-73.574	dB

	Switch 6		Switch 8		Unit
	IN-Port1	IN-Port2	IN-Port1	IN-Port2	
S11	1.6092		1.7066		SWR
S12	-2.0626	-1.9275	-2.166	-2.0336	dB
S21	-1.912	-1.7725	-2.0111	-1.8611	dB
S22	1.3073	1.2	1.3322	1.2533	SWR
S12 with switch Off	-81.379	-74.52	-78.484	-78.999	dB

Table 6. Measured scattering parameters for Switches 3 and 5

Specification	Value	Unit
Freq. Range	0 - 5	GHz
Isolation S12	75	dB
VSWR, in	1.3	SWR
VSWR, out	1.3	SWR
Insertion loss	1.8	dB

Table 7. Vendors' specification for the switch

The conclusion from the above measurements is that even if the data fluctuate around the specifications (see Table 7). The performance of the switches will be acceptable in the breadboard environment. If problems are encountered during the breadboard verification the impact of those tolerances should be revisited.

4. Low Power Amplifier (LPA)

The Low Power Amplifiers are manufactured by RF Bay Inc and one is shown in Figure 34. The model is the LPA-4-14 and it is optimized for small signals. Measurements were done on two LPAs labeled 1 and 2 (see Table 8). The specification values from the vendor's documentation are shown in Table 9.

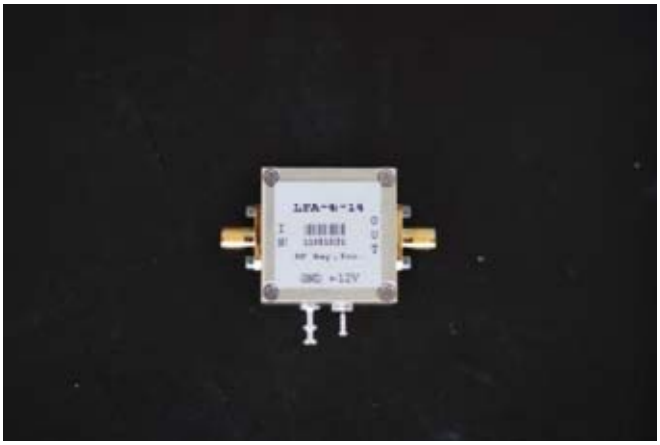


Figure 34. LPA-4-14, RF BAY Inc.

	LPA 1	**LPA 2**	Unit
	IN-Port1	IN-Port1	
S11	1.4382	1.4326	SWR
S12	-23.77	-23.014	dB
S21	17.416	17.554	dB
S22	1.2376	1.2563	SWR

Table 8. Measured scattering parameters for LPA1 and LPA2

Specification	Value	Unit
Freq. Range	0.1 - 4	GHz
Isolation S12	-22.5	dB
VSWR, in	1.5	SWR
VSWR, out	2	SWR
Gain S21	18.2	dB

Table 9. Vendor's specification for the LPA

The Low Power Amplifier exceeds the specification in isolation, and in both input and output VSWR. However the gain is reduced by the amount of 0.5 dB. The slightly lower gain will not have an impact for our purposes.

5. Low Noise Amplifier (LNA)

The Low Noise Amplifiers are also from RF Bay Inc. The model chosen is a LNA-2700 (see Figure 35).

Figure 35. LNA-2700, RF BAY Inc.

The frequency range for this amplifier is between 2.2 GHz and 3.2 GHz, and the values of the specifications are interpolated from the vendor's plots for the LNA. Both the measured and specification values are shown in Table 10. Both of the Low Noise Amplifiers exceed the vendor's specification in all fields.

	LNA 1	**LNA 2**	Unit
	IN-Port1	IN-Port1	
S11	1.3913	1.3079	SWR
S12	-56.623	-56.623	dB
S21	24.985	24.923	dB
S22	1.2975	1.3661	SWR

(a)

Specification		Unit
Freq. Range	2.2 - 3.2	GHz
Isolation S12	-55	dB
VSWR, in	2.5	SWR
VSWR, out	1.5	SWR
Gain S21	23	dB

(b)

Table 10. (a) Measured scattering parameters for LNA1 and LNA2 and (b) vendor's specifications

E. SUMMARY

In this chapter a verification of previous work was performed. Further developments in implementation due to problems that arose during this process are addressed in Chapters IV and V. The major of those problems is the LPA position and the use of a constant gain instead of the AGC function of the demodulator board. Due to the fact that new T/R modules were to be built, all the scattering parameters of the hardware components were measured to provide reference for measurement and troubleshooting later in their development.

In the next chapter, the design process for the two new T/R modules is presented. The final hardware configuration is displayed and the signal levels in the modules are calculated, measured, and depicted in the corresponding schematics. Furthermore, the synchronization process is analyzed and the LabVIEW implementation is described in detail. In the last section of the chapter, the waveform capability of the hardware is investigated, and the several candidate radar waveforms are displayed.

IV. HARDWARE AND SOFTWARE IMPLEMENTATIONS OF NEW SOLUTIONS IN THE DDAR SYSTEM

A. BACKGROUND

In order to verify previous work and to continue with the implementation of new solutions, two new T/R modules are needed. After the experience of working with rigidly built boxed T/R modules that did not allow easy access for modifications, the decision was taken to build two new modules in a more spread configuration. These modules provide a much more flexible arrangement for investigating architectural modifications and making measurements.

The synchronization process is developed and implemented in an automated way to provide phase coherence of the modules. Furthermore, in this chapter the various waveforms that can be generated from the DDAR system are investigated.

B. THE BREADBOARD T/R MODULES

1. Overview

As mentioned before, the new breadboard T/R modules were built to provide easy access to measurement points and also to allow reconfiguration of the components. The most difficult part of building the new modules was the manufacturing of the cables. Both their electrical connectivity and the microwave propagation characteristics were checked. One drawback is the size of the modules (i.e., the surface area covered). However, after their operation is verified and validated they can be re-assembled in smaller packages (boxes).

2. T/R Module Redesign

When Grahn performed the demonstration of the two modules, he experienced trouble with the circulator isolation and leakage signals. The problem occured both in the Synchronization mode (SYNC mode) and the Normal mode (NORM mode). When

operating in SYNC mode, the leakage of the LO signal through the circulator (from port 3 to port 2) could not be suppressed more than 21 dB which can be seen in Figure 36. This resulted in unpredictable phase errors. In the NORM mode similar behavior was observed due to the circulator. The LO feedthrough signal was leaking through the TX/RX circulator, also shown in Figure 36.

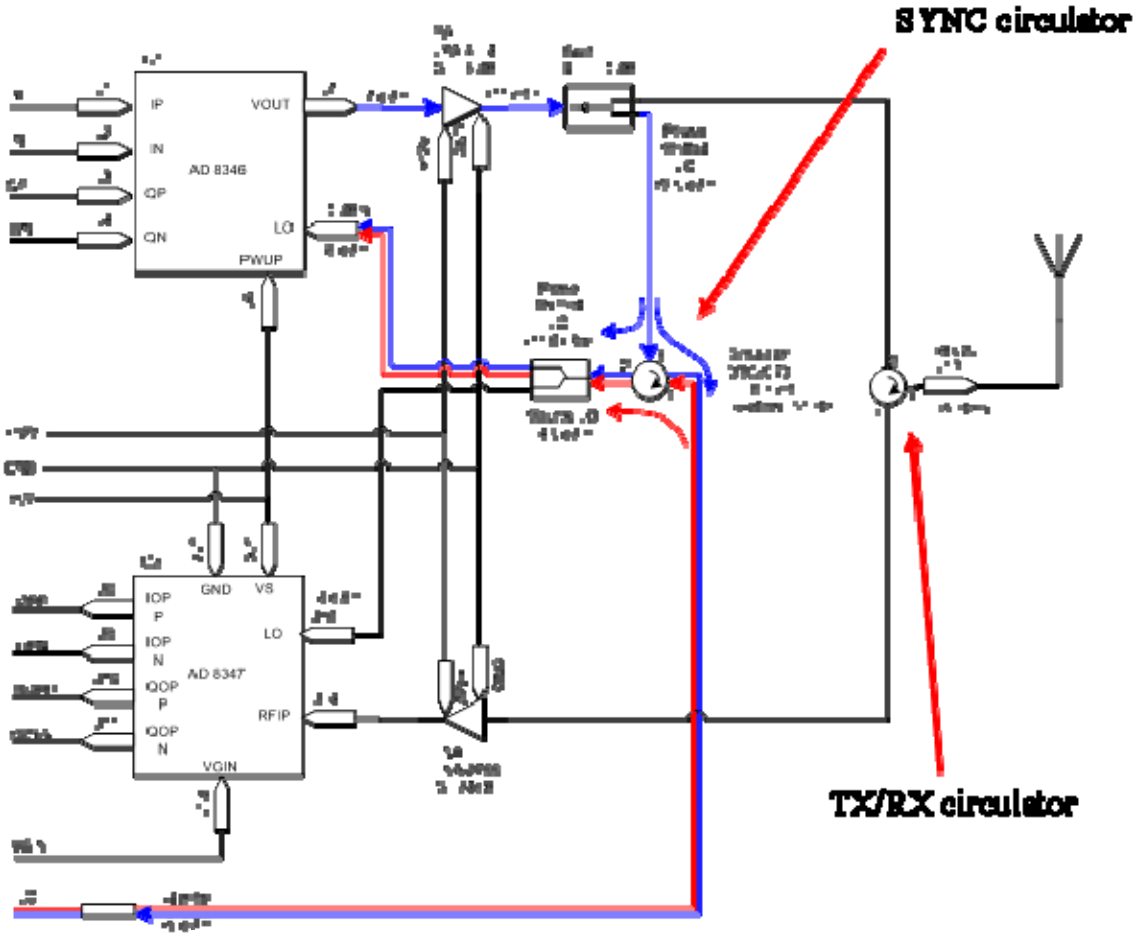


Figure 36. Circulator leakage problems (from [12])

The received signal from the target is estimated to be far less than the feedthrough signal. In a separate project Grahn evaluated the scattering parameters for a power divider (splitter) and examined how it would be possible to implement this solution in the T/R

modules. Although that the difference in isolation between the splitter and the circulator was measured by Grahn and he reported that the splitter had a 9.5 dB higher isolation between the ports, our measurements show that the isolation for both components is 20 dB.

The result of Grahn's work and his suggested solution is presented in Figure 37 and Figure 38. Note that the TX/RX circulator in Figure 36 has been replaced by a switch.

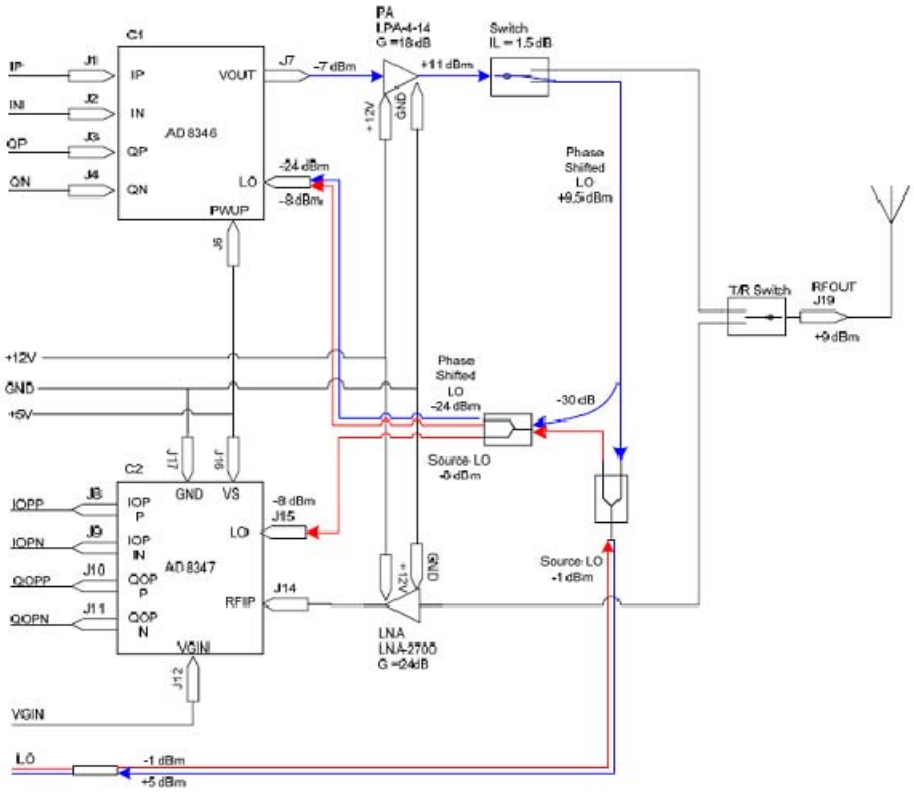


Figure 37. New T/R module design schematic of SYNC mode (from Grahn's unpublished note)

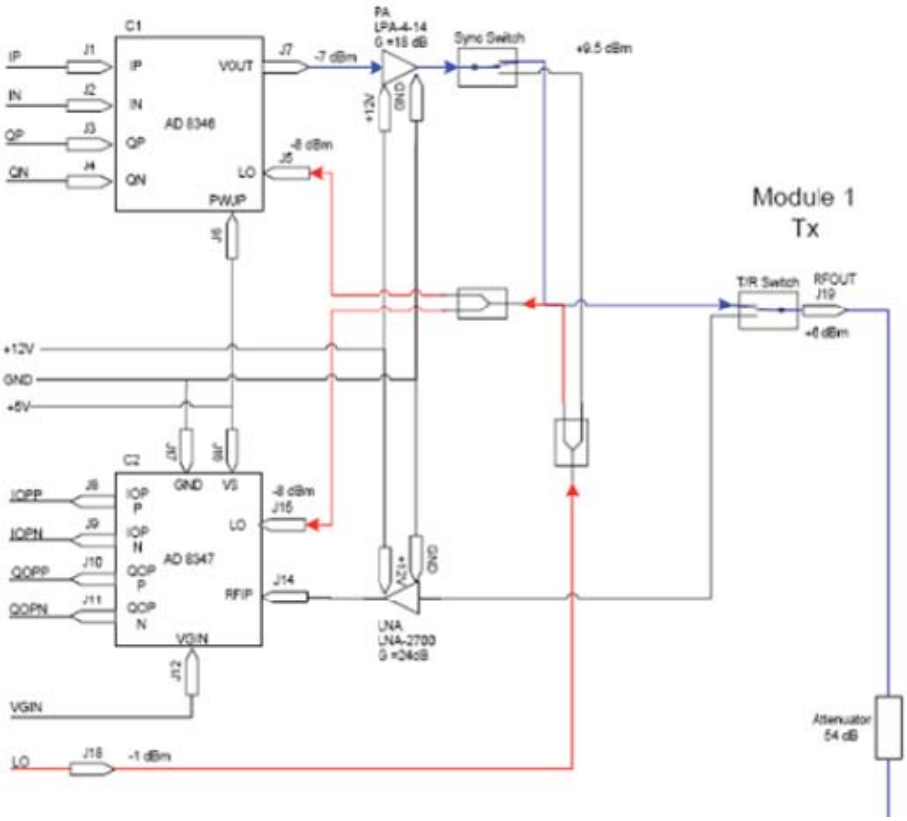


Figure 38. New T/R module design schematic of NORM mode (from Grahn's unpublished work)

The benefit of using switches is that the isolation between the output ports is approximately 80 dB, which far exceeds the performance of the circulators. Starting with this solution the two new T/R Modules were built, and they are shown in Figure 39 and Figure 40.

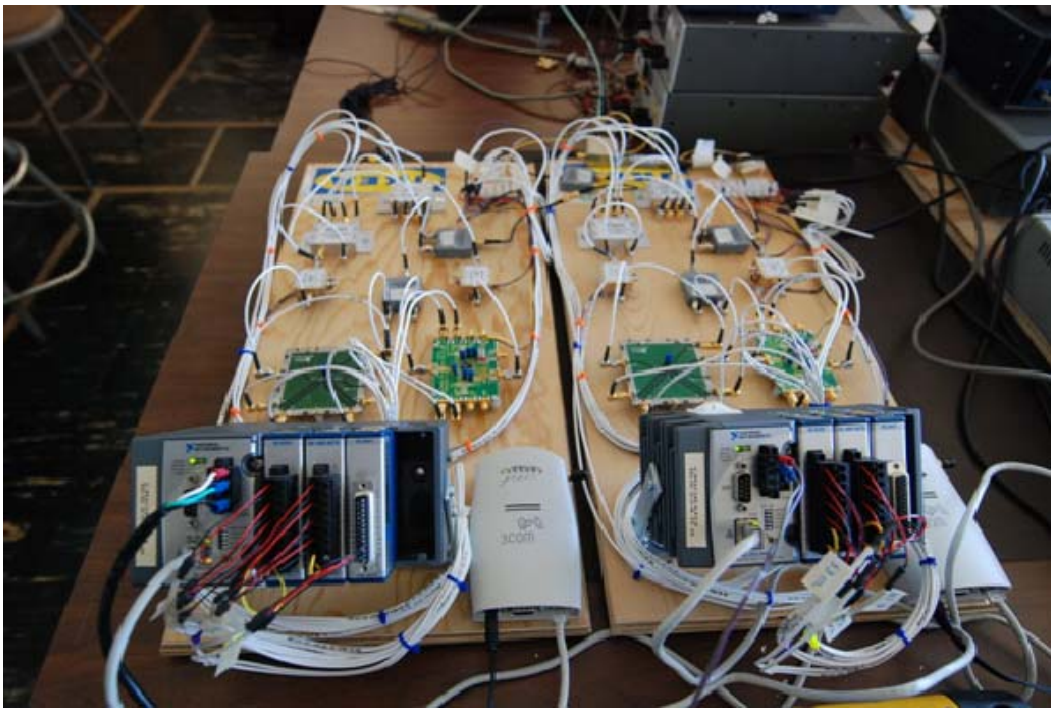


Figure 39. The two new breadboard T/R modules

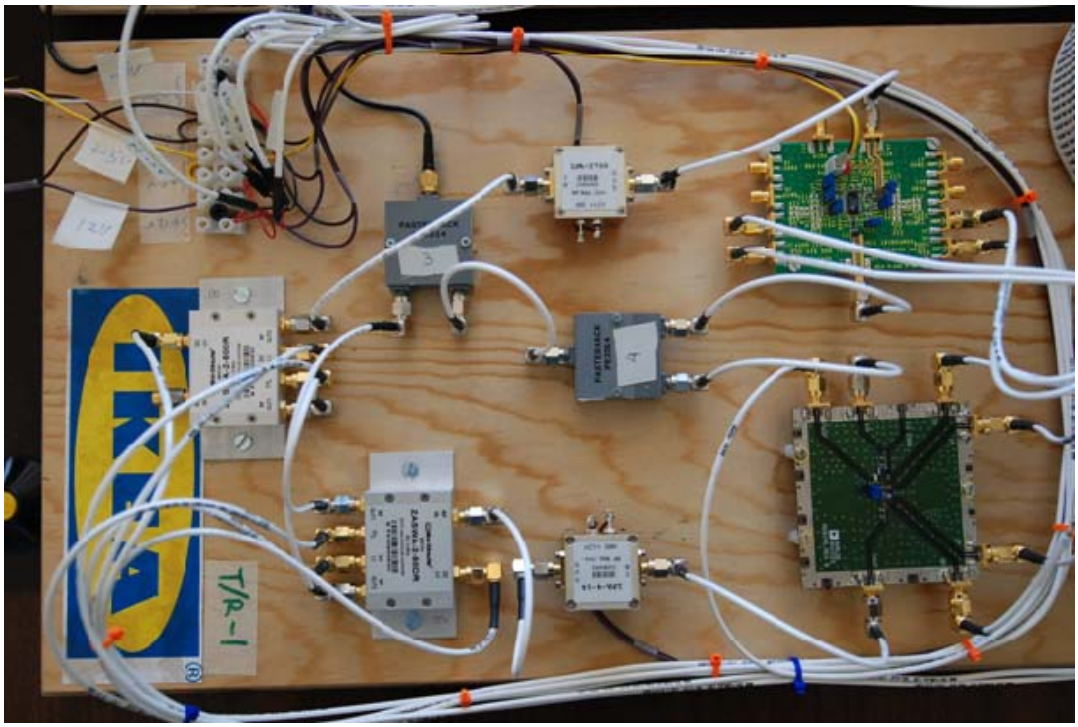


Figure 40. Detailed view of the RF section of T/R module 1

3. Calculated Signal Power

In order to verify the effectiveness of the modification, new power calculations were performed. The scattering parameters already measured were used to provide the maximum possible accuracy. The only exception is the VOUT power from the modulator board. The value used for this component was taken from the vendor's data sheet [22]. The AD8346 modulator board is designed to operate in the range spanning from 800 MHz to 2.5 GHz. The output power from the board is 0 dBm at 800 MHz and drops rapidly above 1.1 GHz as shown in Figure 41. The power is as low as -14 dBm at 2.4 GHz.

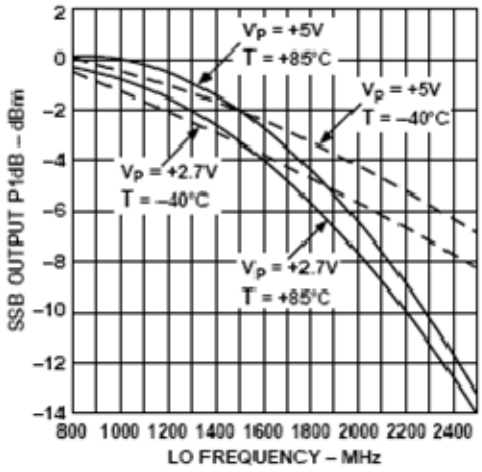


Figure 41. AD8346 output power from [22]

The calculated power values for the SYNC mode are shown in Figure 42 and for the NORM mode the values are shown in Figure 43. The main signals are shown as solid lines, and the leakage and secondary signals are dashed.

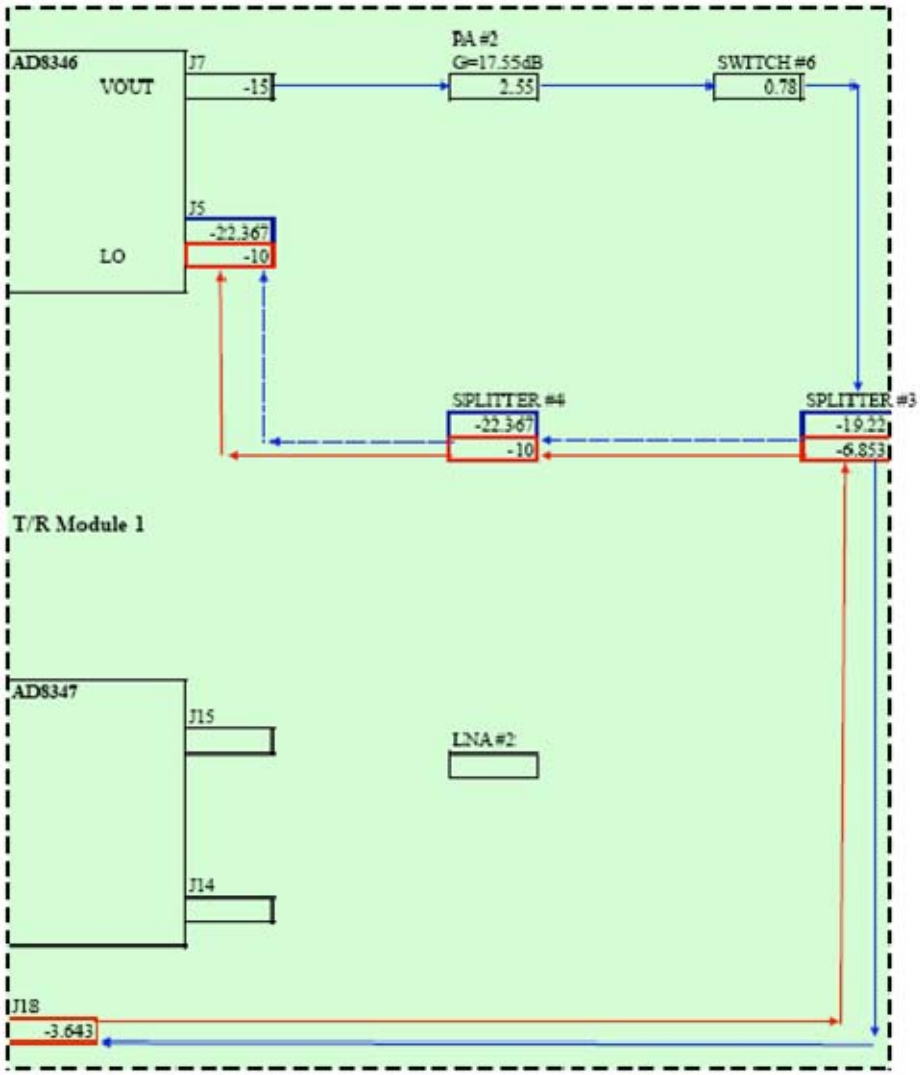


Figure 42. Power calculations in SYNC mode on T/R module 1 [dBm]

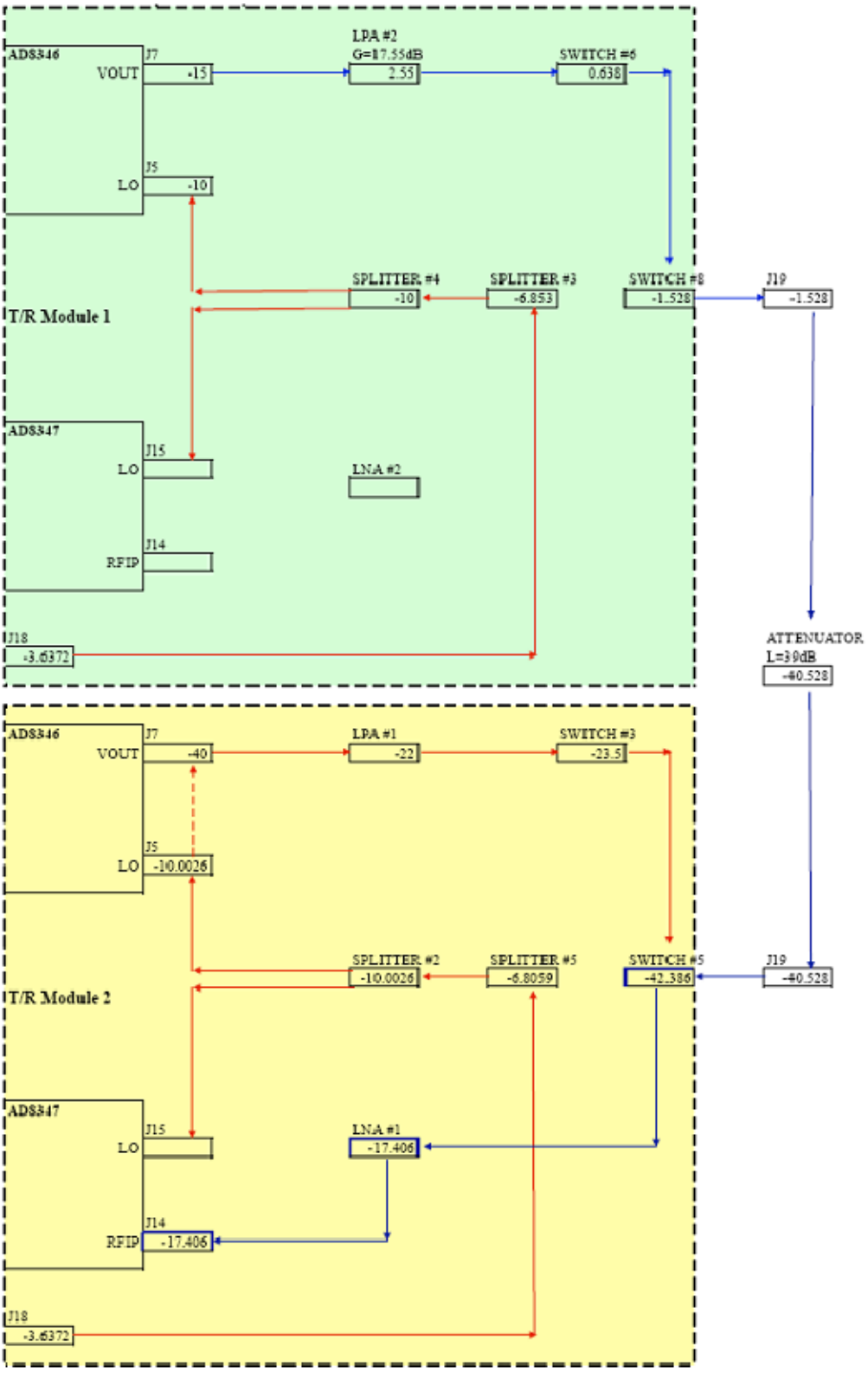


Figure 43. Power calculations in NORM mode [dBm] with T/R module 1 transmitting and T/R module 2 receiving

4. Measured Signal Power

The only inconsistency between the calculated values and the measured values is the output from the modulator board. The specification value of -14 dBm could not be reached, even when the voltage levels from the I- and Q-channels were set to the maximum limit (2.5 V or 5 V peak to peak). The measured power values for the SYNC mode are shown in Figure 44 and the measured power values for the NORM mode are given in Figure 45.

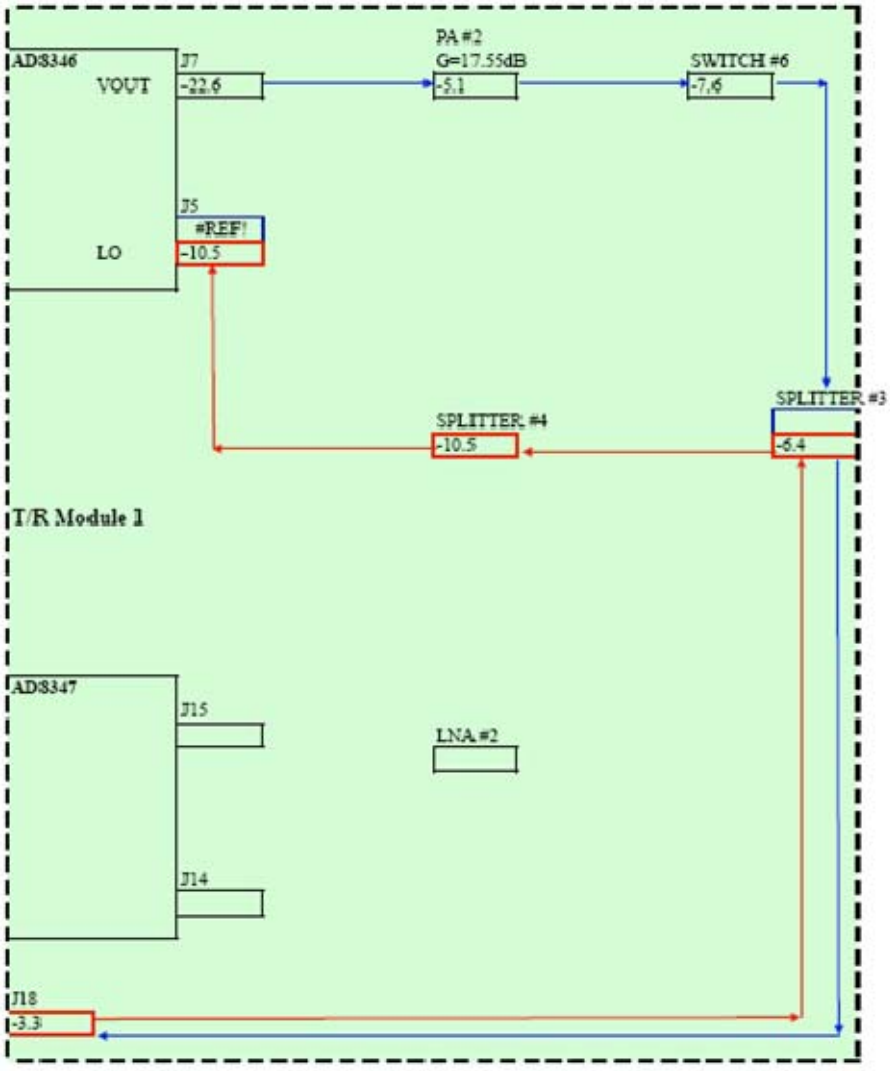


Figure 44. Measured power SYNC mode on T/R module 1 [dBm]

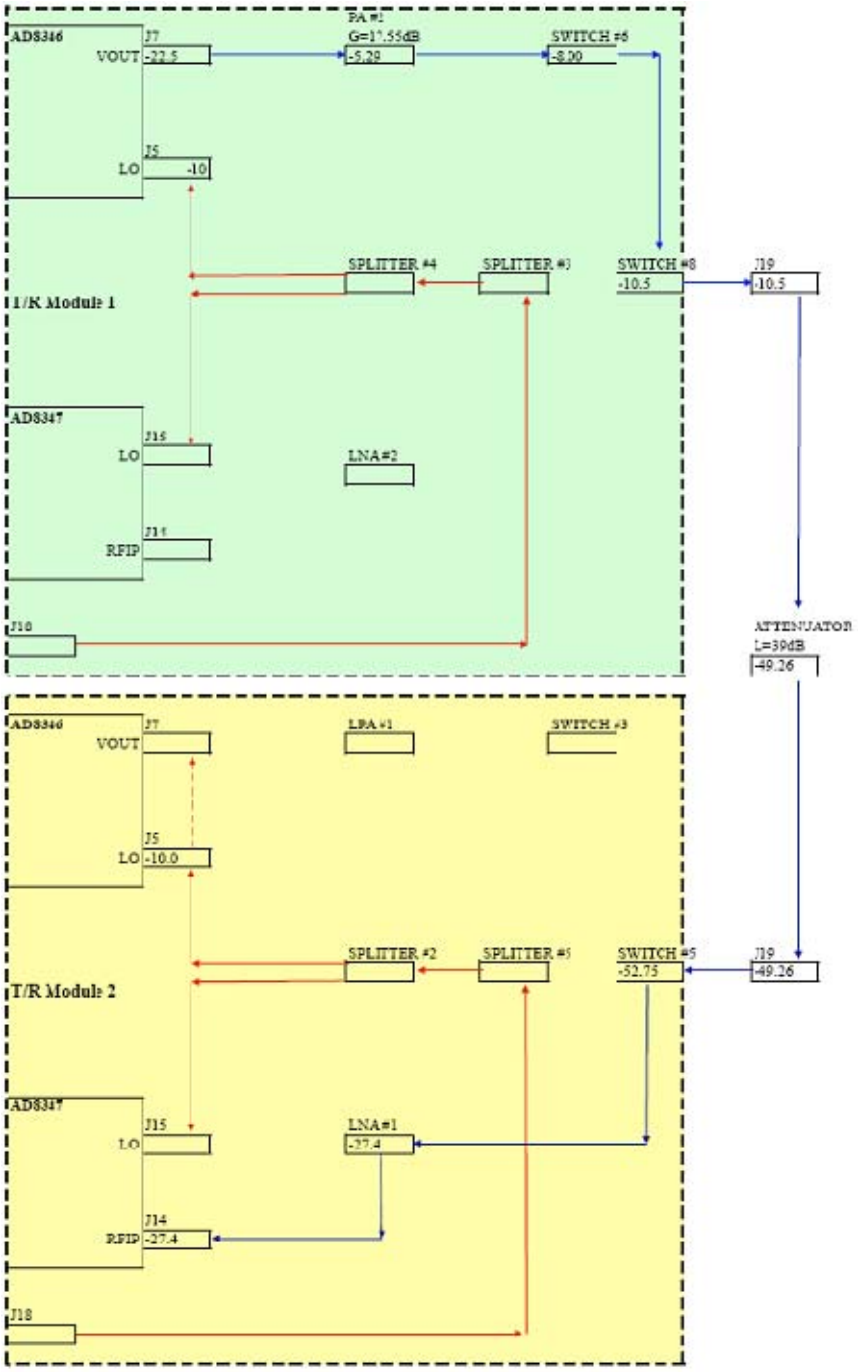


Figure 45. Measured power NORM mode [dBm] with T/R module 1 transmitting and T/R module 2 receiving

These power levels will be examined in more detail in Chapter V, where the results from the synchronization circuit will be analyzed.

C. SYNCHRONIZATION PROCESS AND SOFTWARE DEVELOPMENT

1. Overview

In order to synchronize the phase of the T/R modules, a modification of the "brute force" technique proposed by Loke [9] is implemented. In theory, the proposed technique should work efficiently because only one global minimum is present in a complete period. In particular, it occurs when the signals experience destructive interference. When this minimum is found, the phase shift is determined and there is no need to complete the scanning through the rest of the cycle. However, real measurements have shown many local minima within a period. Therefore, one cannot just increase the phase until a minimum has been reached, because of the risk of being trapped within a local minimum.

This thesis proposes to scan through a complete period. Although someone could argue that this technique is inefficient, it will provide correct results by avoiding trapping within a local minimum. Also, phase steps of 5 or 10 degrees are sufficient for the desired accuracy, so stepping through 360° goes quickly. When the scanning is complete, the data are stored in an array and can be further processed. The global minimum can be located and the associated phase shift can then be assigned to the corresponding module. The total voltage samples from the detector that are processed within a period are subject of trade off between accuracy and efficiency. The phase synchronization requirement is found to be 20 to 30 degrees [7]. However, the notch can occur over a very short phase interval, on the order of 10 degrees. To balance both of the requirements, the decision to take samples every 10 degrees was made.

a. Data Structures

The measurements and processing are done in LabVIEW. The only data structures needed for the implementation of the synchronization process are two parallel 1x36 arrays. One array holds the phase values, and the other holds the voltmeter measurements. Notice that the array that holds the phases is used to index the

measurements. In this way, when the minimum voltage value is located, the corresponding phase can easily be extracted from the other parallel array by using the same index.

b. Synchronization Algorithm

The algorithm used in the synchronization process is presented in the following top-level pseudo code format:

```
<Enter SYNC mode>

Set the synchronization switch of the reference T/R module
to SYNC

For all the other T/R modules

      Set the synchronization switch of the T/R module to
      SYNC

      Set the phase assigned to the modulation board to
      zero

      While the phase assigned to the modulation board is
      less than 360

            Get the voltmeter measurement and store it in
            an array

            Increase the phase by ten degrees

      Find the minimum value in the array

      Store the phase that corresponds to the minimum value

      Add 180 degrees to the stored phase value

      Apply a modulo of 360 degrees to the previous phase
      value

      Assign that phase to the modulation board

      Set the synchronization switch of the T/R module to
      NORMAL

Set the synchronization switch of the reference T/R module
to NORMAL

<Exit SYNC mode>
```

2. LabVIEW Implementation

The synchronization process was bundled with the existing LabVIEW program developed by Noris [13] to demonstrate the transmission and reception of signals to and from the T/R modules. They both are located in the project "DDAR.lvproj." This is installed in the controller computer used in the set up. The DDAR software can be operated in NORM or SYNC mode directly from the "Main_2.vi" front panel. The documentation of how to operate the program is included in Appendix A. It is advised that the reader opens the corresponding VIs on the computer alongside with reading the text. The following sections describes the "DDAR.lvproj" elements.

a. DDAR Operating Mode

The two controls that are used to select the operating mode of the DDAR are shown in Figure 46.

Figure 46. DDAR modes

- "DDAR_MODE" enumerated list

It displays all the functions that the DDAR can perform up to the current development stage. Namely, it contains the "NORM" selection for normal operation, the "SYNC" selection for the phase synchronization of the T/R modules, and the "OFF" selection to gracefully exit the program. The enumerated list is shown in Figure 47.

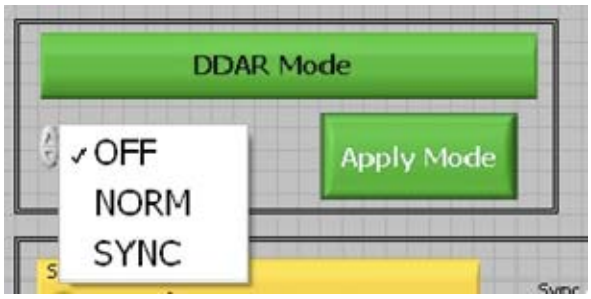


Figure 47. "DDAR_MODE" enumerated list

- "Apply_mode" pushbutton

After making the appropriate selection on the "DDAR_MODE" enumerated list, the "Apply_mode" pushbutton must be pressed in order for the selected mode to be in effect. Indicators, on the respective mode areas show which mode is executing at the given time.

b. Synchronization Process Interface

The interface of the synchronization program is developed to make it easy and intuitive for the user. The visible controls and indicators are illustrated in Figure 48.

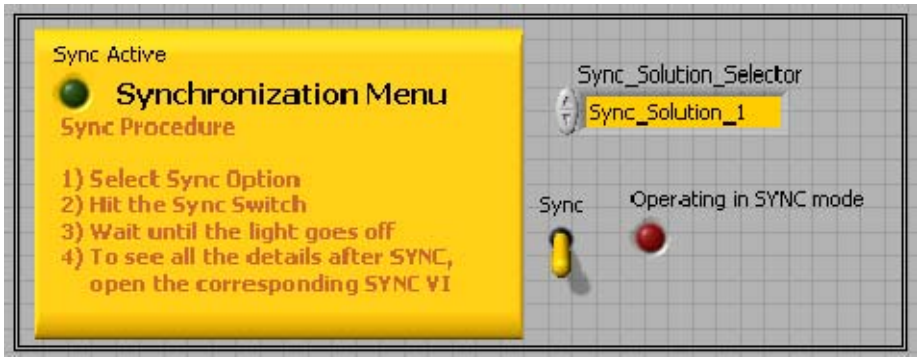


Figure 48. Synchronization process GUI

- The "Sync" switch

The "Sync" switch initiates the synchronization process. Its mechanical action is set to switch until released. This allows multiple synchronizations within a given

operating time of the DDAR. Once the switch is selected, the corresponding synchronization solution is executed. Notice that the desired solution should be set before hitting the “Sync” switch through the “Sync_Solution_Selector” as described in the next section.

- The “Sync_Solution_Selector” list box

The “Sync_Solution_Selector” list box offers two options for the synchronization of the T/R modules:

i. The “Sync_Solution_1” is used to efficiently synchronize the existing two -element set up. It is faster to execute and involves just one function call. In particular the “Sync_Solution_1.vi” is called. When it finishes, it returns program control to “Main_2.vi.”

ii. The “Sync_Solution_2” is used to synchronize a set up of two or more T/R modules. It is written in a way to easily allow addition of an arbitrary number of modules for synchronization. It will be handy when the design is expanded to eight elements. As the function calls are considered, the “Sync_Handler.vi” is called first. This, in turn, sequentially calls the individual synchronization VIs. Upon completion it returns control to “Main_2.vi.”

- The “Operating_in_SYNC_mode” indicator

The purpose of the “Operating_in_SYNC_mode” indicator is to provide visual confirmation that the DDAR is operating in the SYNC mode. If the synchronization involves more than one element, the indicator will be off when all of the modules have been synchronized. Caution of should be taken not to make changes in the controls when the indicator is on. The limitations and possible interactions are explained in the global variables section.

c. Structure of the “DDAR.lvproj”

The directory structure of the “DDAR.lvproj” is provided in Figure 49. A brief description of the functions or virtual instruments (VIs) that are relevant to the

synchronization process will follow. Note that the "Global_Variables," the "Main" and the "SubVIs" folders reside in the controller or host computer. The contents of the "FPGA_VIs" folder are executed in the corresponding FPGA device.

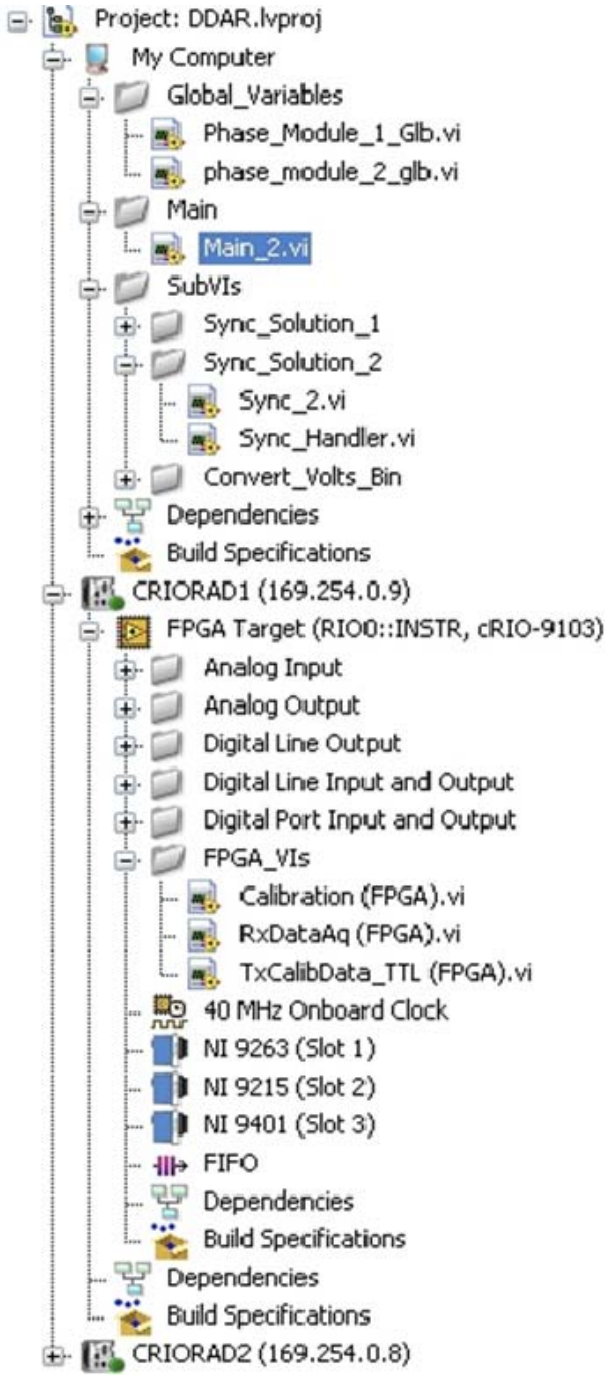


Figure 49. "DDAR.lvproj" project directory structure

d. Functions Involved in the Synchronization Process

The functions or VIs that are contained in the project and are relevant to the synchronization process are grouped in folders which contain relevant VIs. The listing that follows describes the VIs that lie in each folder.

- Main

"Main_2.vi" is the main function that contains the TX and RX demonstration as well as the synchronization interface. This is the main function of the DDAR program. All other functions and VIs are called from within the "Main_2.vi." In this function the TX/RX demonstration and the synchronization process occupy the two most significant cases of the LabVIEW case structure. If the case that corresponds to the SYNC is selected, the framework of the synchronization process is executed and is shown in Figure 50. There is a one to one correspondence to the synchronization GUI as described earlier in this section.

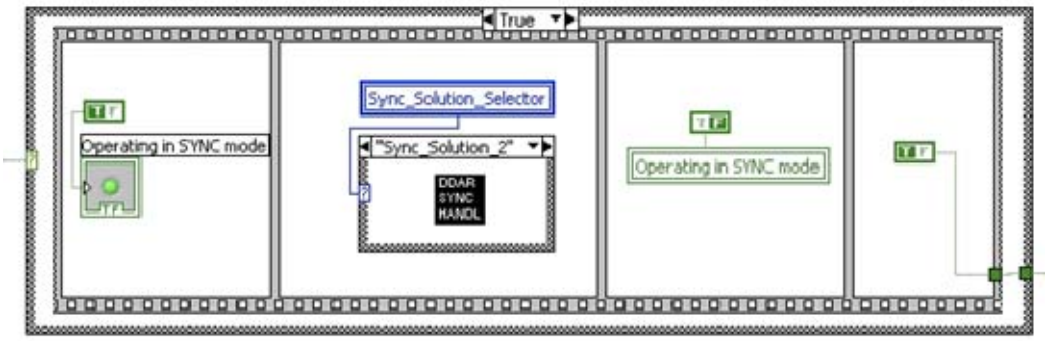


Figure 50. Synchronization framework in the "Main.vi"

- Global variables

There are two global variables in the project. Each global variable is assigned a corresponding VI. The purpose of those variables is to allow different VIs to be able to have access to them. The need to assign a phase value from the

synchronization process to the modulation board of the T/R module that is under synchronization, involves modifying the phase of the module as defined in the TX part for that module in the main program.

Note that while the global variables provide the fastest and most efficient way to share resources among different processes when used with caution, they can be source of bugs extremely difficult to track. One should be aware that if they are not used carefully, they could cause race conditions between the competing processes, which try to alter it at the same time. Because this is a critical point, all the competing processes are documented and highlighted in this document.

As a last comment, in LabVIEW terms, a global variable is set to “Read mode” when a value is assigned to that global variable. In the same manner, “Write mode” means that the global variable is providing its value to another variable or expression.

The “Phase_Module_1_Glb.vi” defines the phase of the T/R module 1 to be a global variable. The variable can now be controlled from a number of different VIs. Note that each global variable is defined in its own VI. The “Phase_Module_1_Glb.vi” is used to pass the phase of the T/R module 1 to the synchronization process in order for the module under synchronization to be assigned with the correct phase. It is also used in write mode in the “Main_2.vi” to inform the user about the phase setting in the T/R module 1. In conclusion, it is only used in write mode throughout the project so no other VI will ever try to change it. ***However, if there is an intentional change on the “Phase_Module_1_Glb.vi” while the synchronization process executes, the results will be erroneous. This behavior is due to the fact that the reference phase for the module under synchronization is changed during the time that samples are taken.***

The “Phase_Module_2_Glb.vi” defines the phase of T/R module 2 to be a global variable. The variable is used in write mode in the “Main_2.vi” and in read mode in the synchronization VIs. It is used when the synchronization VIs are finished with the calculation of the correction phase that should be assigned to T/R module 2. When completed, this phase value is returned to the modulation board. This is done with the use

of “Phase_Module_2_Glb.vi” in read mode. In particular, when the synchronization process executes, if the “Phase_Module_2_Glb.vi” is changed on purpose, it will have no effect on the synchronization integrity. As soon as the synchronization completes, the phase that will be assigned to the “Phase_Module_2_Glb.vi” will be the result of the synchronization process. ***Therefore, caution should be exercised because any changes in “Phase_Module_2_Glb.vi” during the synchronization process will be discarded.*** It is safer to follow the instructions on the “Main_2.vi” and wait for the “Operating in SYNC_mode” light to switch off before making any changes.

- Sync_Solution_1

This function implements the synchronization of the two-element demonstration set up currently in use. It is the most efficient solution for that purpose but is difficult to expand to more elements. The function must ensure that T/R module 2 has its transmission channel active. This ensures that the “Sync” switch is active. This happens because it is operated through the TX while loop of T/R module 2. Also, the NI-9401 of each of the T/R modules is successively set to SYNC mode. When the process is completed, they are both set to NORM mode. The algorithm implementation in LabVIEW will be presented in the “Sync_Solution_2” as the latter is going to be the solution that will be used in the future.

- Sync_Solution_2

This is a more modular approach developed to accommodate the expansion to an eight element demonstration set up. Upon the completion of the construction of the additional six elements, the “Sync_Solution_2” will be able to perform the synchronization of the eight elements. This solution will be presented in a top down fashion.

The sequence of events is the following. When the “Sync” switch is set to true and the “Sync_Solution_Selector” is set to “Sync_Solution_2,” the “Sync_Handler.vi” is called. This intermediate function serves as the synchronization manager. The synchronization function of each T/R module is sequentially called until all

of them are synchronized. It also ensures that for the required time interval of the process, the reference T/R module is set in TX mode and has its synchronization switch set to "SYNC." Once the function terminates, the program control is returned back to the "Main" function.

The actual synchronization of T/R module 2 takes place within the "Sync_2.vi" which is placed within the "Sync_Handler.vi." When more modules are added to the demonstration set up, this section of code can be copied and modified for the new T/R module's address. Then it can be named as "Sync_3.vi" etc, and placed into the synchronization queue. Note that a local variable named "Program_Run_Indicator" is used to control the completion of the two parallel while loops. The sequence used in the "Sync_Handler.vi" to hold the individual synchronization functions of each of the modules is shown in Figure 51.

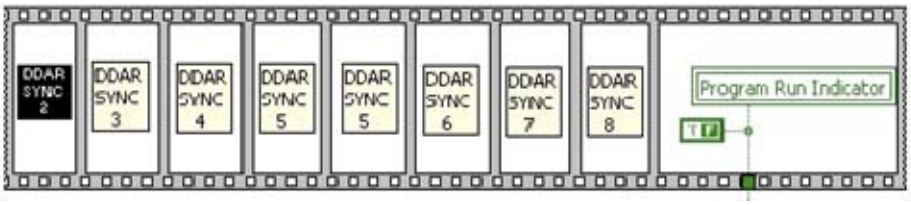


Figure 51. Modular development in the "Sync_Handler.vi"

The "Sync_2.vi" encapsulates the core of the synchronization algorithm as stated earlier. The TX channel of T/R module 2 is forced to be active for the time necessary to collect the required number of samples. The phase is initialized to zero and incremented in steps of 10 degrees and then the corresponding voltmeter reading is recorded. All the data are stored in arrays for further processing. LabVIEW implements this requirement by the use of indexed property on the while loop tunnel. Once the while loop that is used for the data collection is terminated, the temporarily stored data are passed to the actual arrays for further processing. The data acquisition part of the function is shown in Figure 52.

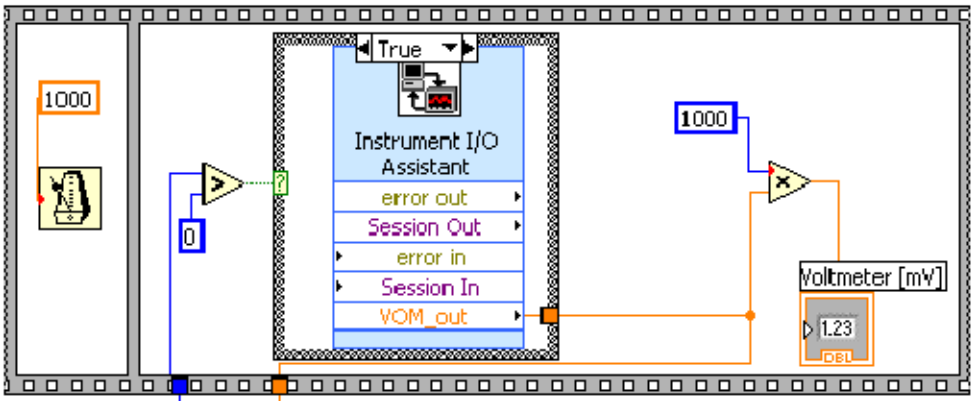


Figure 52. Data collection in “Sync_2.vi”

Next, the core of the synchronization algorithm takes place and it is shown in the LabVIEW block diagram in Figure 53.

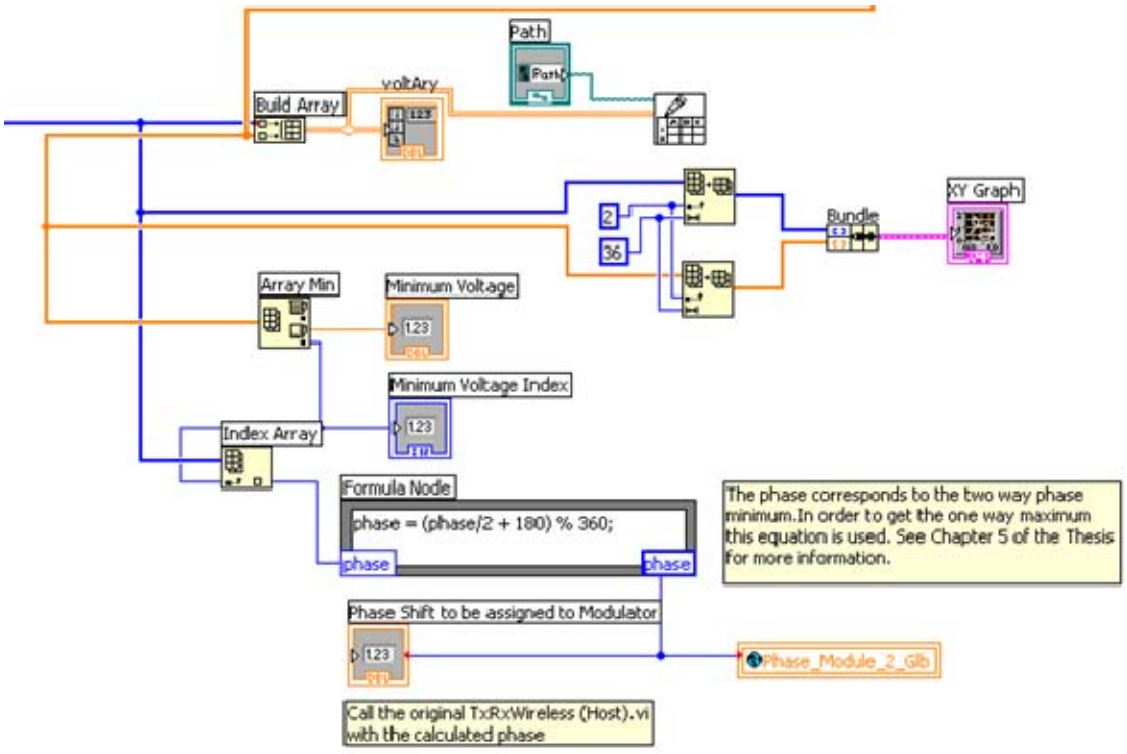


Figure 53. Core of the synchronization algorithm in “Sync_2.vi”

The collected data can be placed in a file specified by the user. The minimum voltage is found, and then the index of that minimum voltage is used to extract the corresponding phase from the parallel array. After that, the measured phase is divided by 2 and 180 degrees is added to that phase, and a modulo of 360 is applied. This is now the phase that is assigned to the modulation board of the corresponding T/R module by the use of the global variable “Phase_Module_2_Glb.vi.”

- FPGA functions

The only function in the FPGAs that had to be altered to accommodate the synchronization process is the “TxCalibData_TTL (FPGA).vi.” The digital output 7 (DIO7) of the NI 9401 is checked at every iteration of the always loop. When found to be on, a voltage of 5 volts is applied to it, allowing the synchronization circuit to operate. The pins that are controlled through that channel are the PIN 25 for the output and the PIN 12 for the common (COM). The modification is shown in Figure 54.

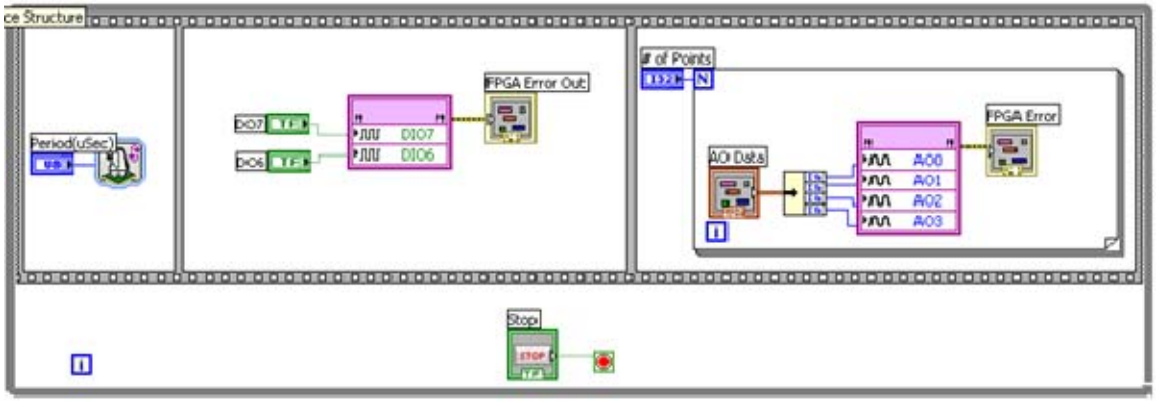


Figure 54. Check for the SYNC switch in the “TxCalibData_TTL (FPGA).vi”

Note that in the NI 9401 properties menu the DIO7 should be configured as “Output.” This is critical because otherwise the switch will not work. The digital output 6 (DIO6) is also added to operate the TX/RX switch, and it can be controlled from the “DDAR.lvproj.” The PINs used on the NI9401 are PIN 23 for the output and PIN 10 for the COM.

D. WAVEFORM INVESTIGATION

1. Overview

The ability to create a variety of different waveforms using the National Instruments equipment being used in the benchtop model was investigated. Furthermore, the ability to control the parameters specific to a waveform were also analyzed. The test bench equipment was used for this experiment. In particular, the NI cRIO-9101 chassis, cRIO-9004 real-time embedded controller, and cRIO-9263 digital-to-analog voltage output module were used to generate the waveforms. The output was set to be from the AO0 channel. The generated waveform was then displayed on the TEKTRONIX TDS 3032B oscilloscope.

The waveforms were generated using LabVIEW. The approach used was to enable the user to define a waveform of his choice by using a look-up table (LUT). The bit-stream of one full period of that waveform would be placed on the FPGA. Eventually, the waveform would be clocked out period after period, as the waveform controller program would always run. This is basically the same procedure used in a direct digital synthesizer (DDS).

2. Equipment Setup

The cRIO-9623 output channel AO0 was used. The line was connected to the terminal 0 and the common was connected to the terminal 1. On the oscilloscope, channel-1 was set to be the input. No external triggering was needed.

3. Project Overview

Five small projects were created to investigate the waveform generating capability and they are listed below:

- Exprerimental.lvproj,
- Pulse_Generation.lvproj,Pulse_Generation(fpga).vi,
- Sine_Wave_Generation.lvproj
- Triangle_Generation.lvproj

- User_Defined_Waveform_Generation.lvproj

A sample structure of the “Experimental.lvproj” is depicted in Figure 55.

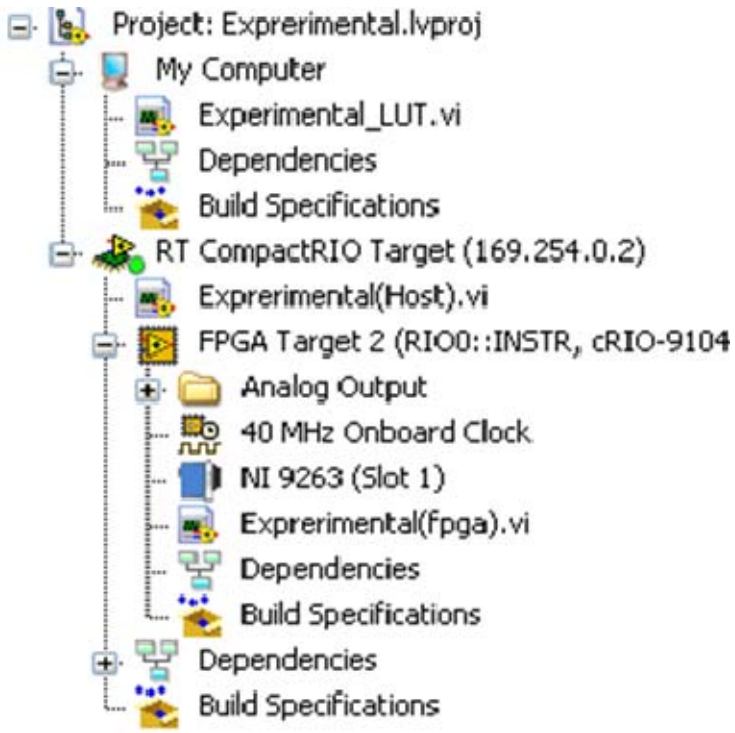


Figure 55. Tree view of the project “Experimental.lvproj”

There are three VIs that reside inside that project and they are described in the following sections.

4. Look Up Table Definition

The “Experimental_LUT.vi” (see Figure 56) is responsible for the generation of the LUT. As it is described in the FPGA program section below, it can be called through the look up table FPGA module as a user defined VI to create a look up table. The particular implementation uses 128 data points, but this can be changed by the user. Clocking speed versus precision of the waveform is the main trade-off. The embedded MATLAB script is used to iteratively assign voltage values to each of the table (actually

an array). Notice that the code directly converts the volts to binary code that is specific to the cRIO-9263 digital-to-analog voltage output module. The formulas used for the conversion are taken from [29]:

$$\text{Code Width} = \frac{\text{Module Voltage Range}}{2^{\text{Module Resolution (bits)}}} \tag{2}$$

$$\text{Binary Code} = \frac{\text{Output Voltage} \times 2^{\text{Module Resolution (bits)}}}{20.0V} \tag{3}$$

The block diagram of the "Experimental_LUT.vi" is presented in Figure 56.

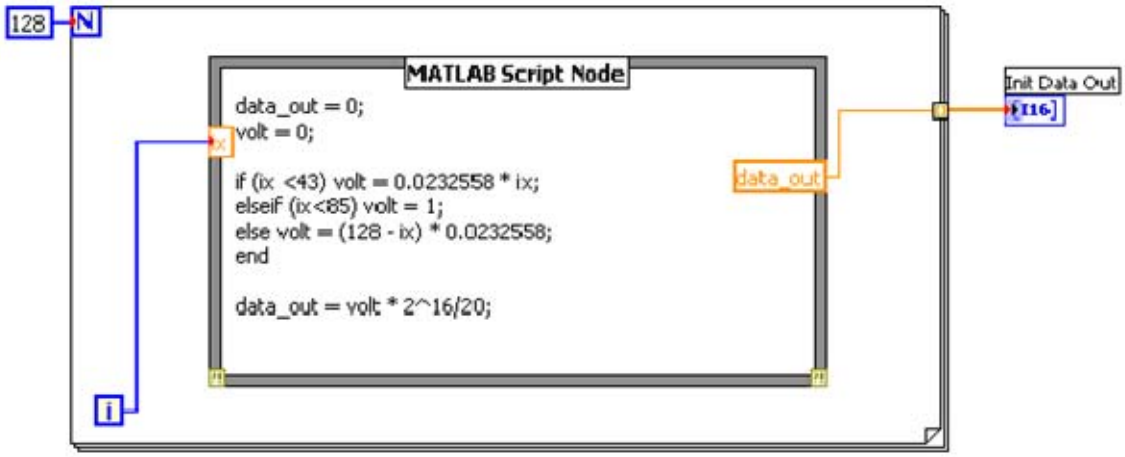


Figure 56. Block diagram of "Experimental_LUT.vi"

Alternatively, one could use the "Convert to Binary.vi" to accomplish the same thing, but the need of calibration data with this approach makes the project less flexible. For demonstration purposes the current approach is sufficient.

5. Controller Program

"Experimental(Host).vi" is the main function and it is deployed to the cRIO-9004 real-time embedded controller. After the bitmap is deployed, the program runs locally on the embedded device. The block diagram of this function is shown in Figure 57.

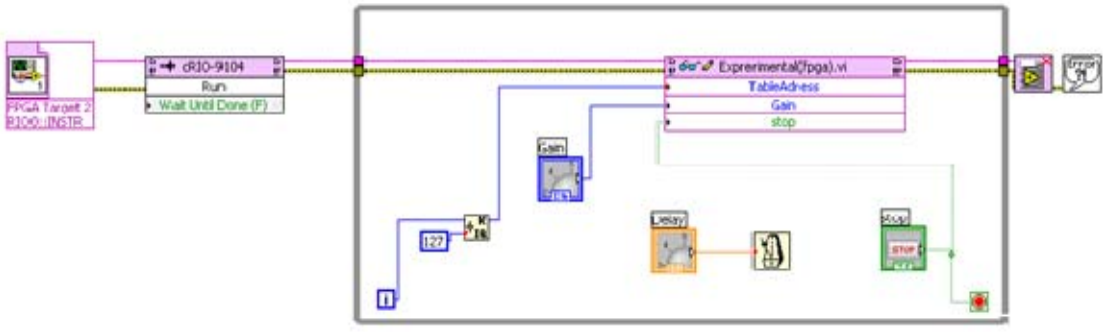


Figure 57. The block diagram of the "Experimental(Host).vi"

The function opens the FPGA program that will be explained in the next section. Then the FPGA program enters an always loop that calls sequentially the LUT entries. At every iteration of the loop, the user can adjust the gain and thus the voltage level of the output waveform. He can also adjust the delay that translates to a frequency setting seen on the oscilloscope. The GUI of the function is shown in Figure 58.

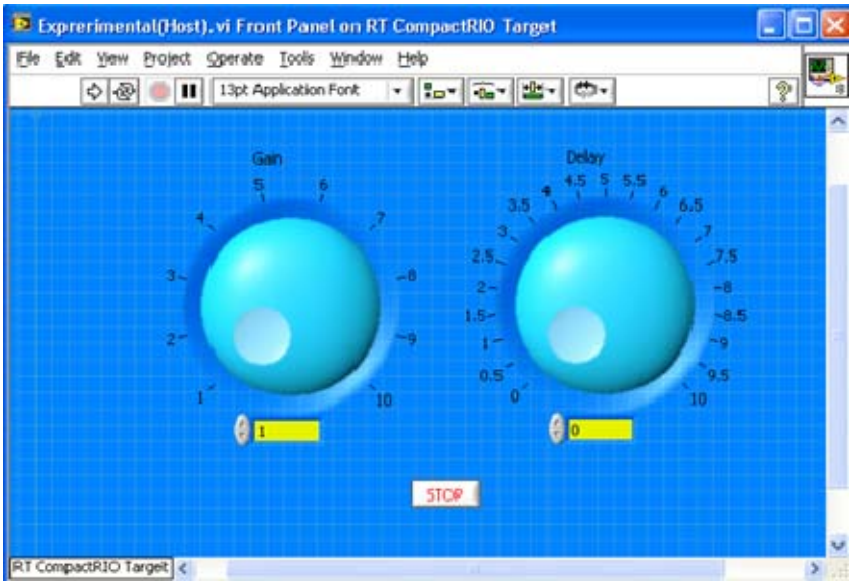


Figure 58. "Experimental(Host).vi" Front panel (GUI)

6. FPGA Function

The program that is "burnt" into the cRIO-9101 chassis' FPGA tiles is "Experimental(fpga).vi." The corresponding block diagram is shown in Figure 59.

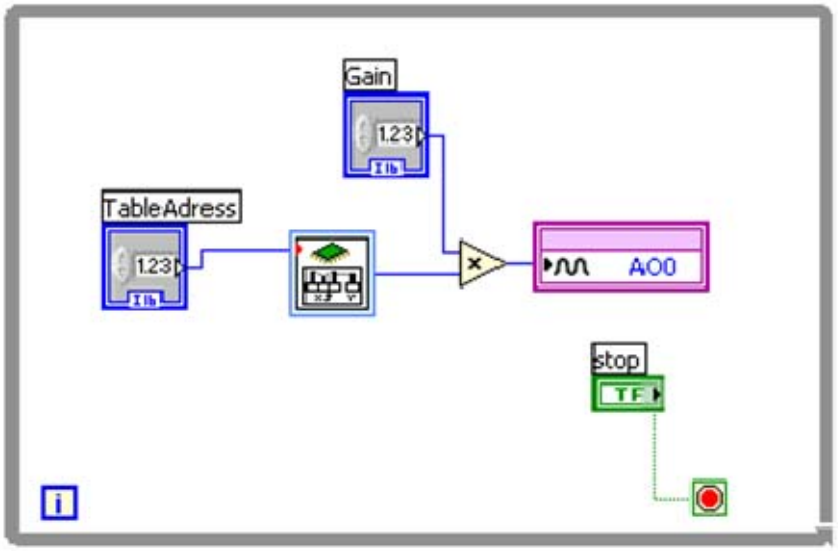


Figure 59. Block diagram of the "Experimental(fpga).vi"

In this function, the table address that is provided by the index of the always loop of the caller "Experimental(Host).vi" is read by the LUT module. After combining the binary code output of the latter with the gain set by the user in "Experimental(Host).vi," the result is then multiplied and forwarded to the analog output channel AO0. This process continues until the user stops the calling function.

The user can change the look up table in the LUT module by selecting the module's properties. This is where the custom "Experimental_LUT.vi" can be used to eventually create the desired LUT. Alternatively, the data-points could be manually adjusted but this would have been impractical.

7. Output

The oscilloscope trace of the output for the above project is shown in Figure 60. The selected waveform consists of a linear increase amplitude section followed by a constant amplitude section and finally a linear decrease amplitude section. The frequency of the waveform is 114 Hz.

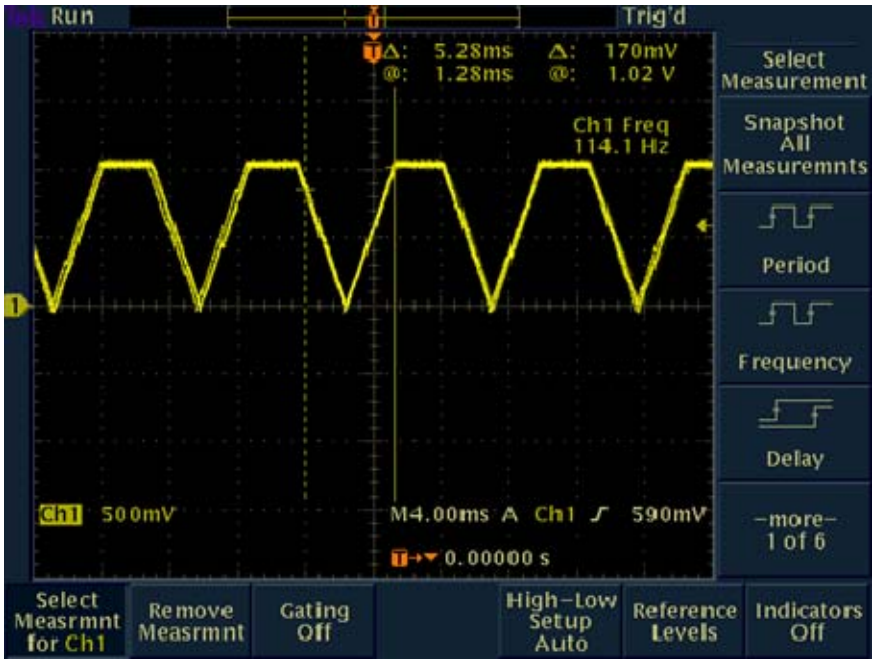


Figure 60. Output of the "Experimental.lvproj" on the oscilloscope

8. Examples

Outputs from the other projects are also shown to illustrate the creation of arbitrary waveforms. In Figure 61 a square pulse with a frequency of 9 kHz is shown. A square pulse but with lower frequency, 123 Hz, is shown in Figure 62. Finally, an example of a triangular waveform is shown in Figure 63.

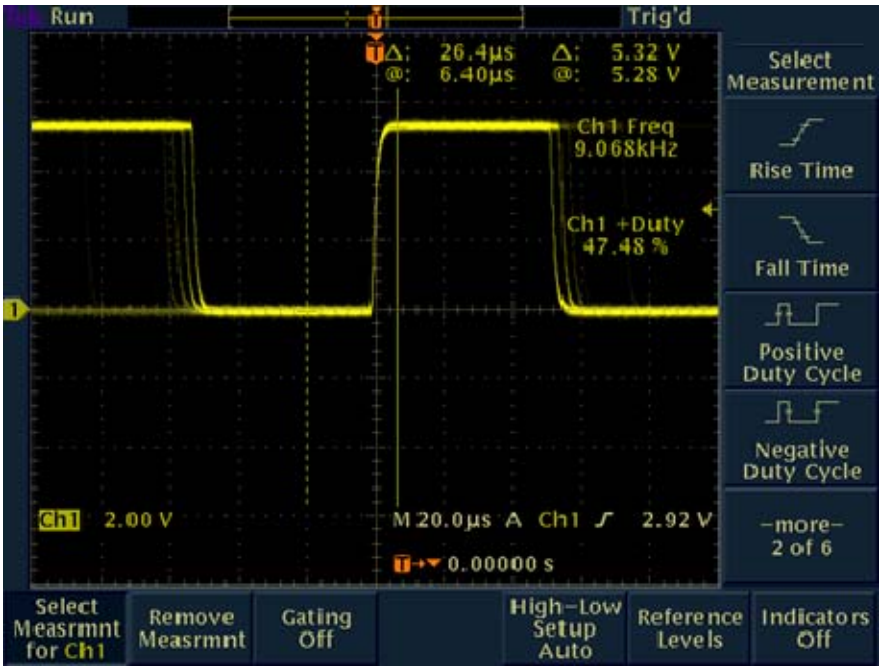


Figure 61. Output of the "Pulse_Generator.lvproj" on the oscilloscope

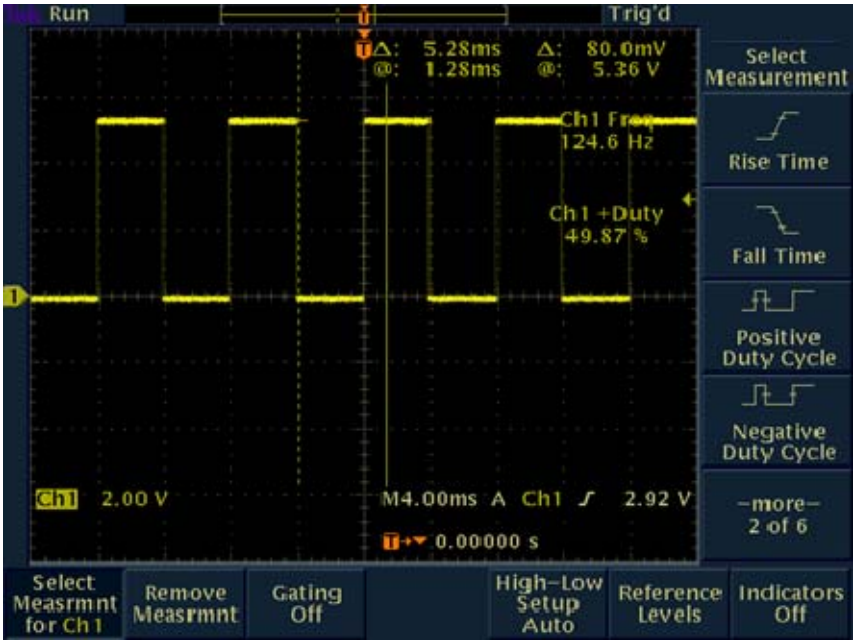


Figure 62. Output of the "Pulse_Generator.lvproj" on the oscilloscope at a lower frequency

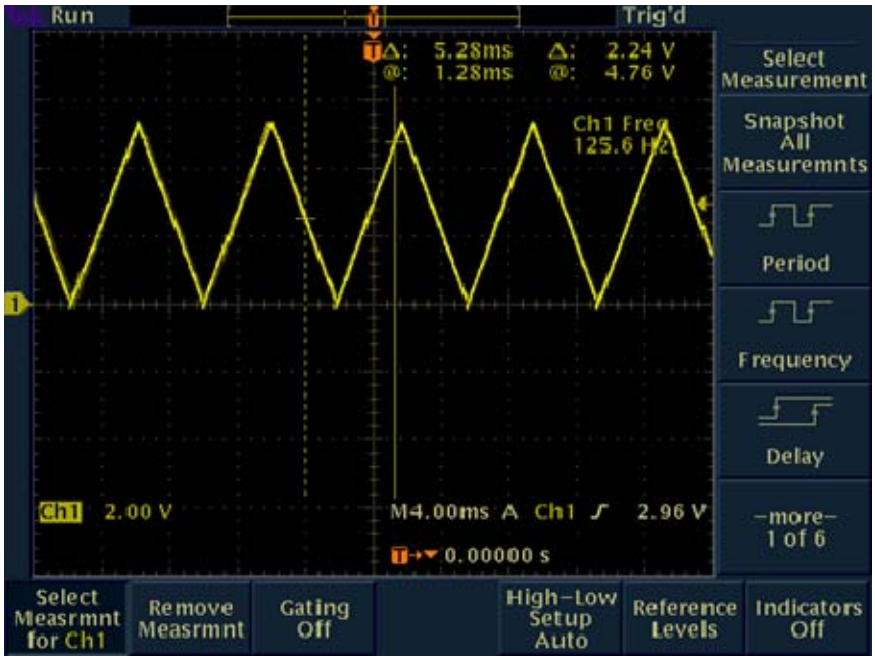


Figure 63. Output of the "Triangle.lvproj" on the oscilloscope

9. Pulse Generation in the DDAR System

The capability of the DDAR system to generate and transmit a pulsed waveform was developed and incorporated into the project. The pulse is generated in the Controller main function. The amplitude of the original signal is modulated to a pulse with a duty cycle equal to 50%. A simple modulo 2 operator is used in the TX module of the T/R module 1 to alter the signal amplitude, as can be seen in Figure 64.

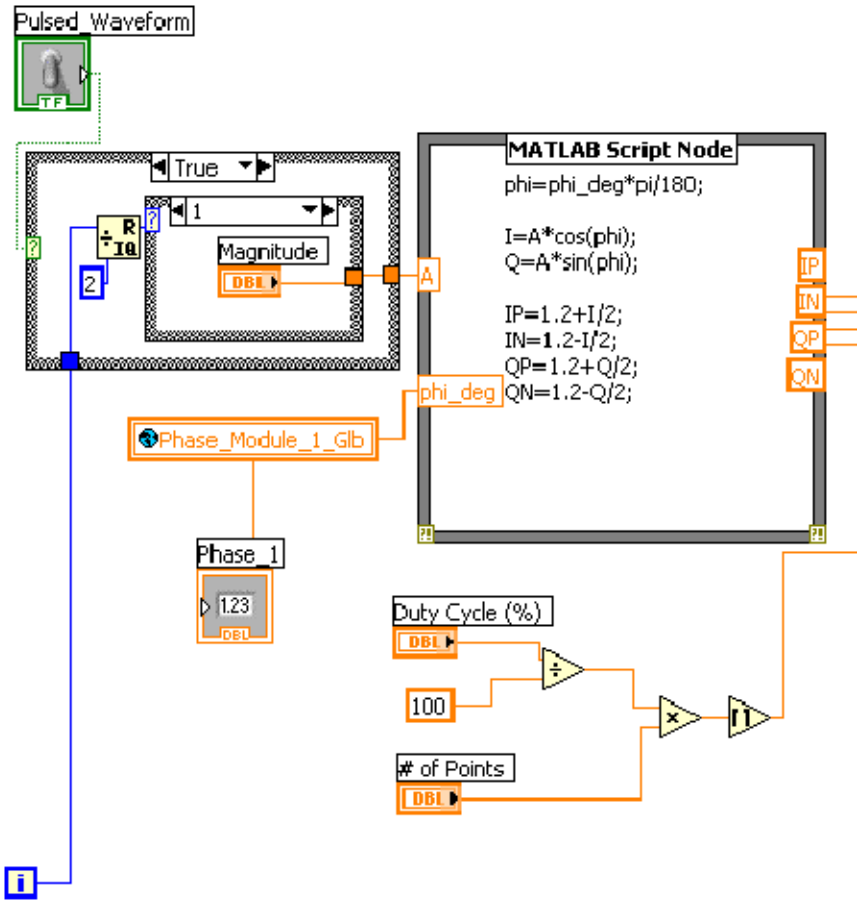


Figure 64. Modified flow diagram of “Main_2.vi” to include the pulse generation

An example run of the “DDAR.lvproj” was performed. The control panel of the program is shown in Figure 65. Notice the blue switch can be selected to output either a pulsed or a continuous signal.

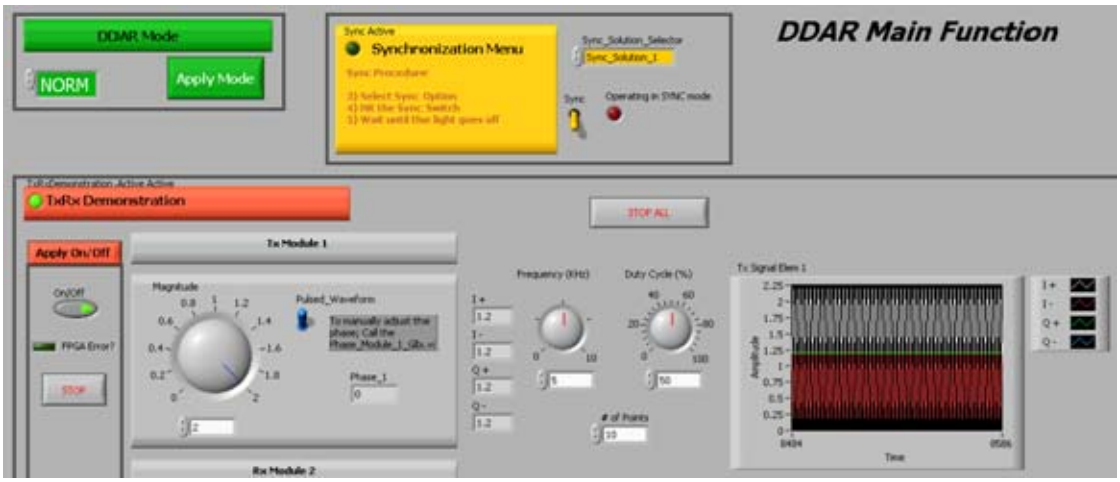


Figure 65. Control panel of “Main_2.vi” including the “Pulse_Waveform” switch

The output from T/R Module 1 was captured with a Tektronix 3032B oscilloscope to verify the correct generation of the pulse. The resulting acquired waveform is presented in Figure 66.

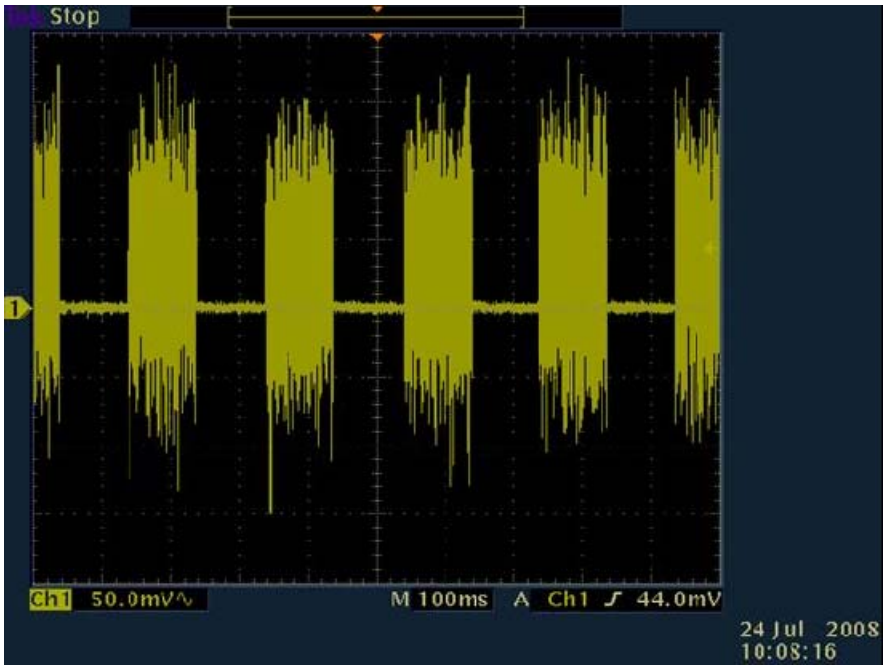


Figure 66. Screenshot of the oscilloscope output, showing the generated pulse train

E. SUMMARY

This chapter started with the description of the building process of the two new T/R modules. They have been designed and developed to address the residual problems of the previous work on the DDAR system. The leakage problems due to the use of circulators were suppressed by the use of switches and splitters. This was later verified by both calculations and measurements of the signal levels throughout the boards. An automated phase synchronization of the T/R modules is implemented through the synchronization process. This will be demonstrated in Chapter V. The chapter concludes with a study of the possible waveforms that can be generated from the real time equipment and a pulse waveform is generated and transmitted by one of the modules.

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V. SYNCHRONIZATION SIMULATIONS AND DEMONSTRATION

A. SYNCHRONIZATION PLAN OVERVIEW

In order to effectively synchronize T/R module 2 to the reference T/R module 1, any phase difference between the LO source and the demodulator LO input must be determined and compensated in the processing. The proposed synchronization process measures the phase difference by transmitting from port A in Figure 67. One of the phases, say ϕ_2, is stepped through 360 degrees. The peak value of the summed signals back at the LO provides the two-way phase shift. The analysis that follows describes how the one-way phase shift can be calculated when the two-way phase shift is known.

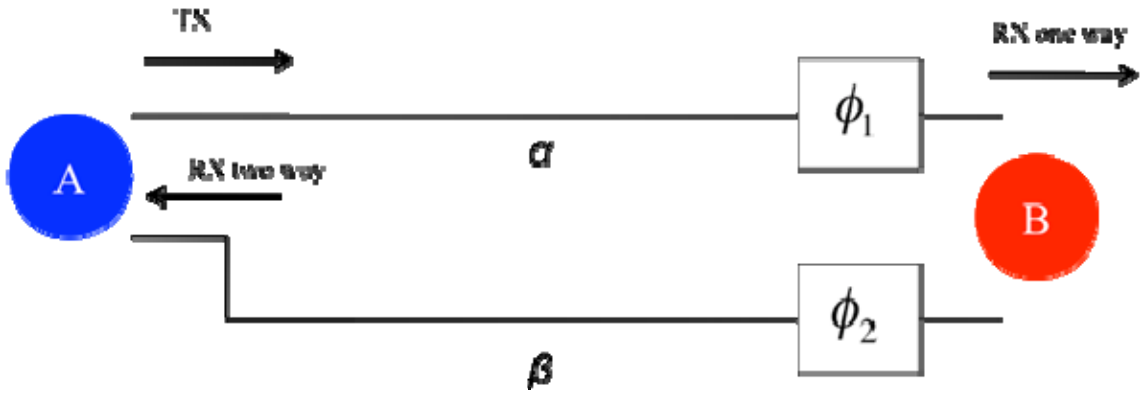

Figure 67. Synchronization concept

Figure 67 displays the synchronization circuit where α is the length between the LO and T/R module 1, β is the length between the LO and T/R module 2, ϕ_1 is the phase shift from T/R module 1, and ϕ_2 is the phase shift from T/R module 2. The phase comparison that is performed at A is the actual two-way phase shift. The one-way phase shift is achieved at B.

For a null to be present at A, the following condition must be satisfied:

$$2(\alpha-\beta)+(\phi_1-\phi_2)=(2n+1)\pi,\ n=...,-1,0,1,... \tag{4}$$

Therefore, the condition for the first null is:

$$2(\alpha-\beta)+(\phi_1-\phi_2)=\pi \tag{5}$$

By substituting

$$\Delta\phi_m=\phi_1-\phi_2 \tag{6}$$

equations (5) and (6) yield

$$2(\alpha-\beta)+\Delta\phi_m=\pi \tag{7}$$

For a null to be present at B, the following condition must be satisfied:

$$\alpha-\beta+(\phi_1-\phi_2)=(2m+1)\pi,\ m=...,-1,0,1,... \tag{8}$$

Therefore, the condition for the first null is:

$$\alpha-\beta+(\phi_1-\phi_2)=\pi \tag{9}$$

By substituting

$$\Delta\phi_d=\phi_1-\phi_2 \tag{10}$$

equations (9) and (10) yield:

$$\alpha-\beta+\Delta\phi_d=\pi \tag{11}$$

From the equations (7) and (11) and by elimination of the α-β common term the one-way phase shift is related to the two-way phase by the following equation:

$$\Delta\phi_d=\frac{\Delta\phi_m}{2} \tag{12}$$

The corresponding one-way maximum is shifted by 180 degrees from the one-way minimum. Therefore the one-way maximum ($\Delta\phi_{d_{\max}}$) can be calculated from the two-way minimum by the following equation:

$$\Delta\phi_{d_{\max}} = \frac{\Delta\phi_m}{2} + \pi \tag{13}$$

B. SYNCHRONIZATION VERIFICATION PLAN

In order to verify the operation of the synchronization circuit, the actual one-way phase shift is measured according to the setup described in the following section. Then the synchronization process is executed and the resulting output is compared with the expected result calculated from a two-way measurement. This process is repeated for different configurations of the synchronization circuit. The demonstration first investigates the synchronization via the usage of a hardwired LO signal. Further demonstrations with wireless setups are to be held as soon as the operation of the synchronization is verified in the hardwired setups.

C. PHASE VERIFICATION "SETUP I"

"Setup I" is shown in Figure 68. In order to get the true phase shift between cables A and B both the modules are set to TX mode and the output at the exit of the modulator boards (RFOUT) is summed with a power meter. Cables C and D are equal phase length. The output at the exit of the modulator board was selected for the measurement because it provides the greatest phase accuracy in the context of the experiment.

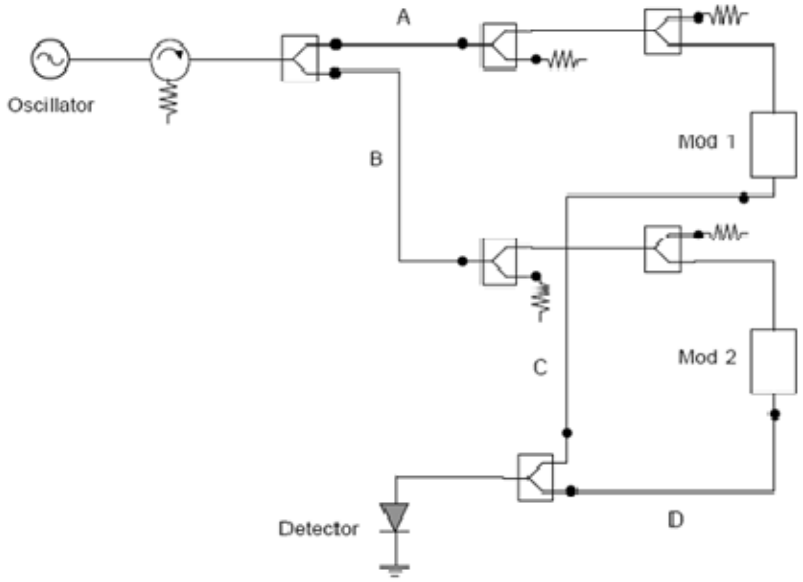

Figure 68. Setup I

The power values are collected while the phase at the reference module is set to zero and the phase at the module under synchronization is stepped over a complete 360 degree cycle in increments of 20 degrees. The maximum of the resulting curve reveals where constructive interference takes place and thus the true phase shift that should be assigned to the T/R module under synchronization.

D. NEW T/R MODULE DESIGN VERIFICATION

In order to verify the correct operation of the synchronization circuit, four different trials are performed, each one of them using a different cable length B for the T/R module 2, while the reference cable A is of constant length throughout the trials. The voltage vs. phase shift is measured for each of the different trials, as described in the previous section. The calculated two-way shift at port A based on a measurement of the shift at port B is compared to the actual measurement at port A. Furthermore, the trials are also repeated after inserting an LPA in the synchronization circuit. Thus, we can have a direct comparison of its effect on the circuit.

1. Synchronization without the LPA in the SYNC Circuit "Setup II"

The configuration of the synchronization circuit that is used in this set up is shown in Figure 69. The LPA is removed from the circuit.

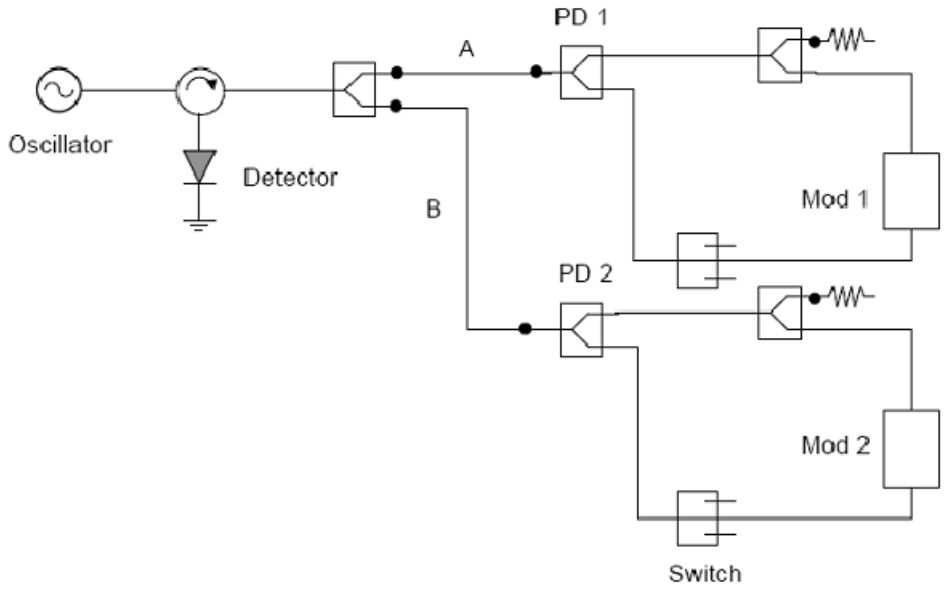

Figure 69. Setup II

a. Cable 1

The measured result from "Setup I" is shown in Figure 70. The peak output is at 0 degrees. The measured two-way voltage from "Setup II" is shown in Figure 71. The calculated one-way compensation phase using equation (13) is 305 degrees. Note that the curve in Figure 71 has some slight deviation from the expected sinusoidal shape.

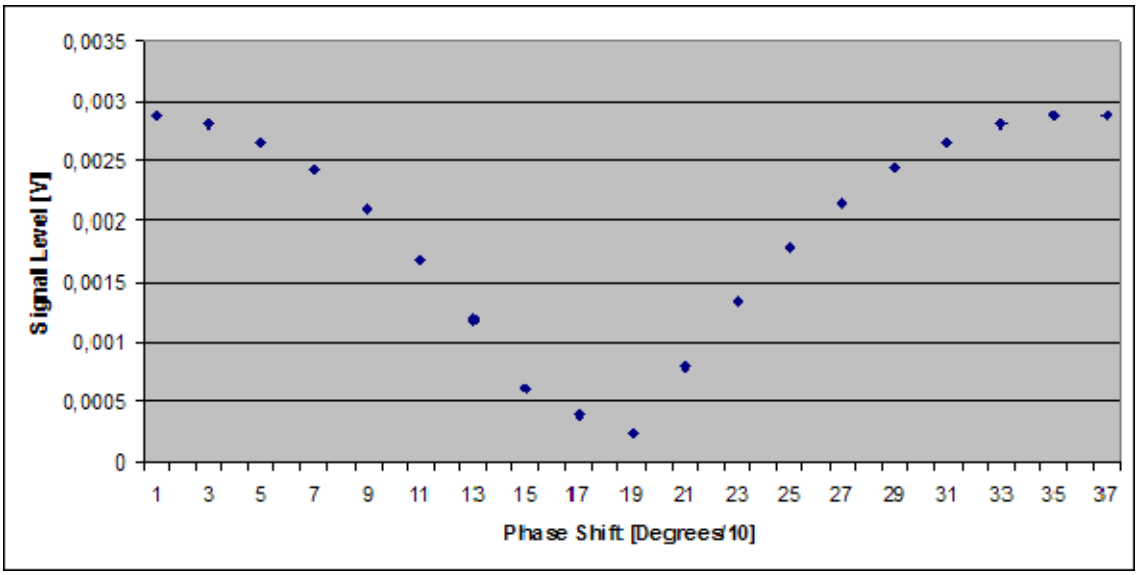

Figure 70. Measured voltage using cable 1, "Setup I"

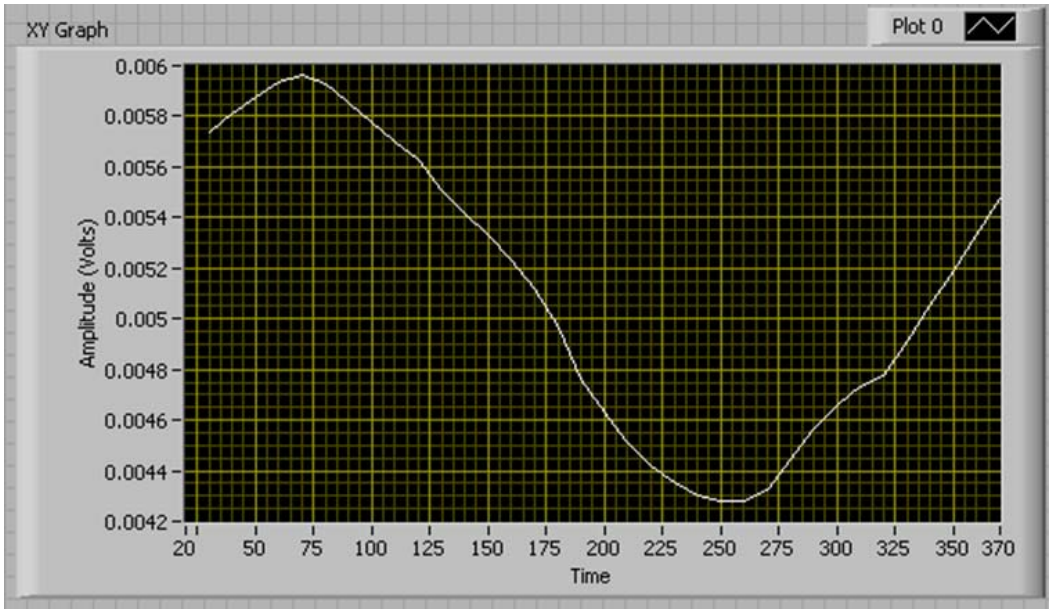

Figure 71. Measured two-way voltage using cable 1 without LPA in the circuit, "Setup II"

b. Cable 2

The measured result from “Setup I” is shown in Figure 72. The maximum is at 100 degrees. The measured two-way voltage is shown in Figure 73. The calculated one-way compensation phase using equation (13) is 240 degrees. Note that the curve in Figure 73 has a major distortion in the area of the minima.

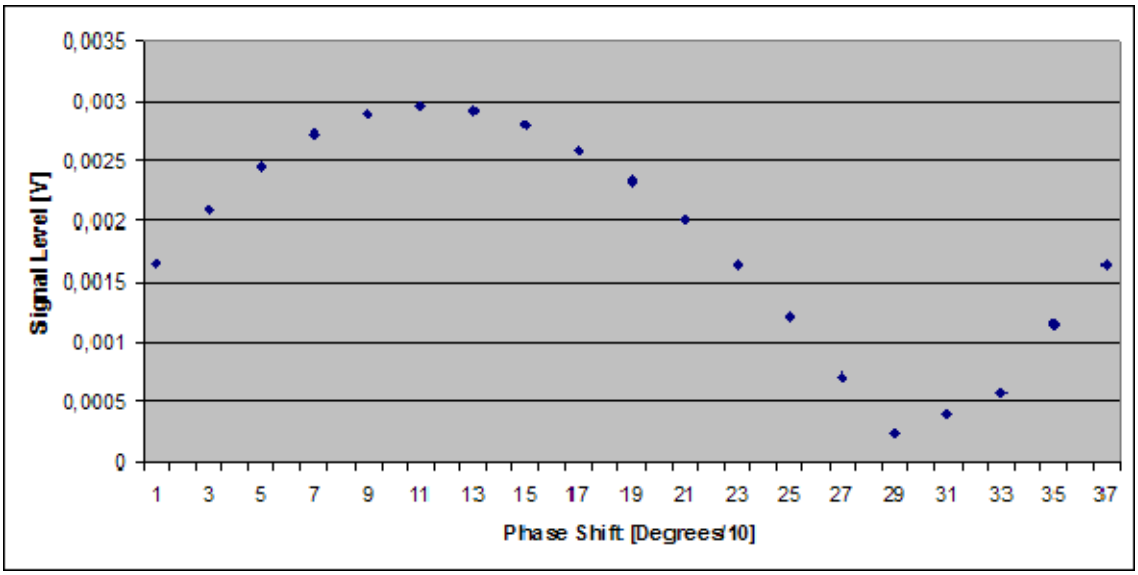

Figure 72. Measured voltage using cable 2, “Setup I”

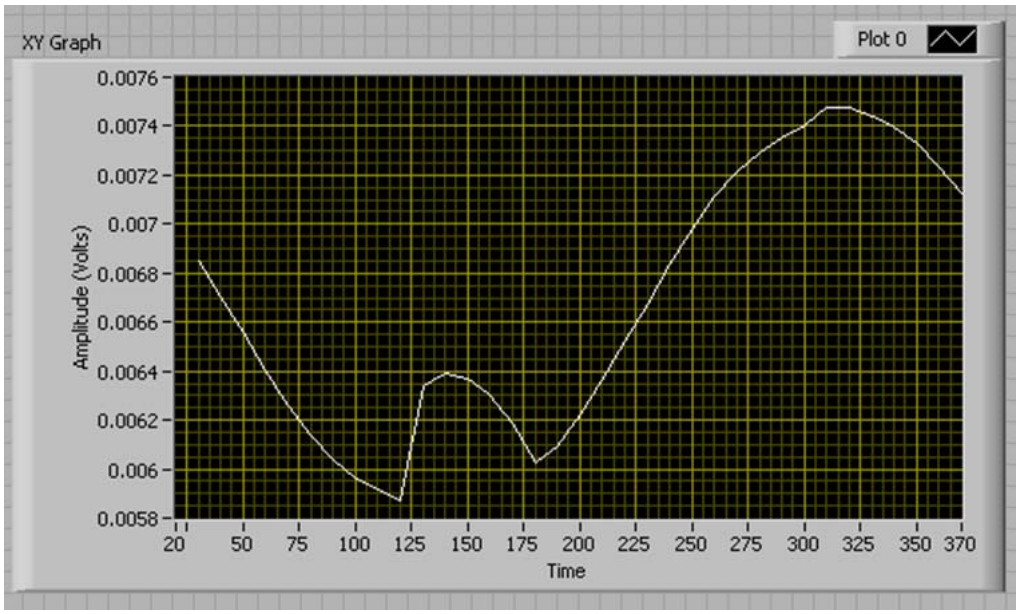

Figure 73. Measured two-way voltage using cable 2 without LPA in the circuit, "Setup II"

c. Cable 3

The measured result from "Setup I" is shown in Figure 74. The maximum is at 340 degrees. The measured two-way voltage is shown in Figure 75. The calculated one-way compensation phase using equation (13) is 320 degrees. Again, the curve in Figure 75 has some distortion when compared to a sinusoid.

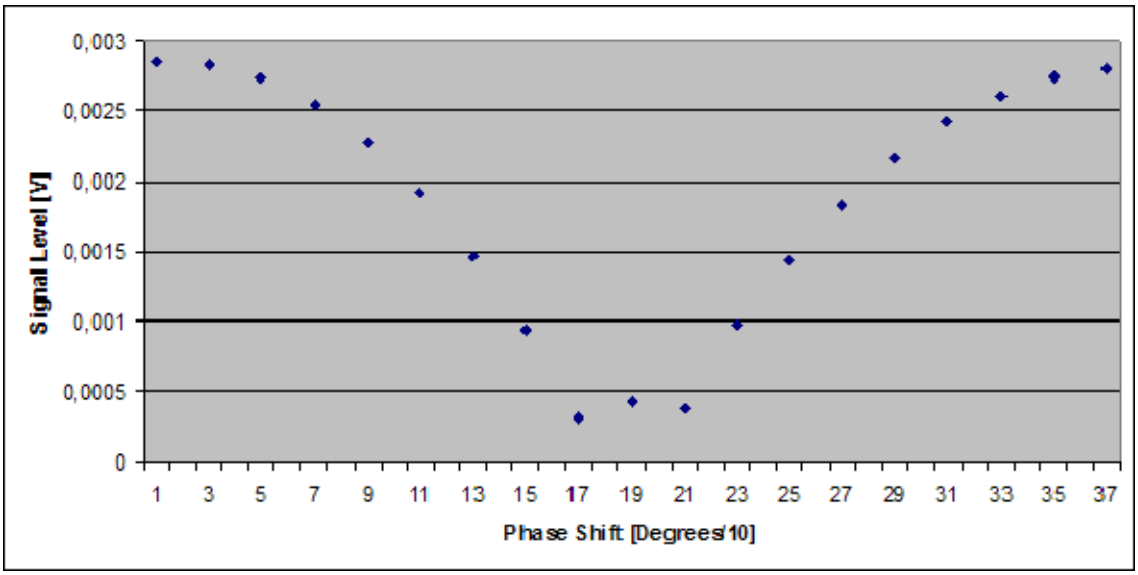

Figure 74. Measured voltage using cable 3, "Setup I"

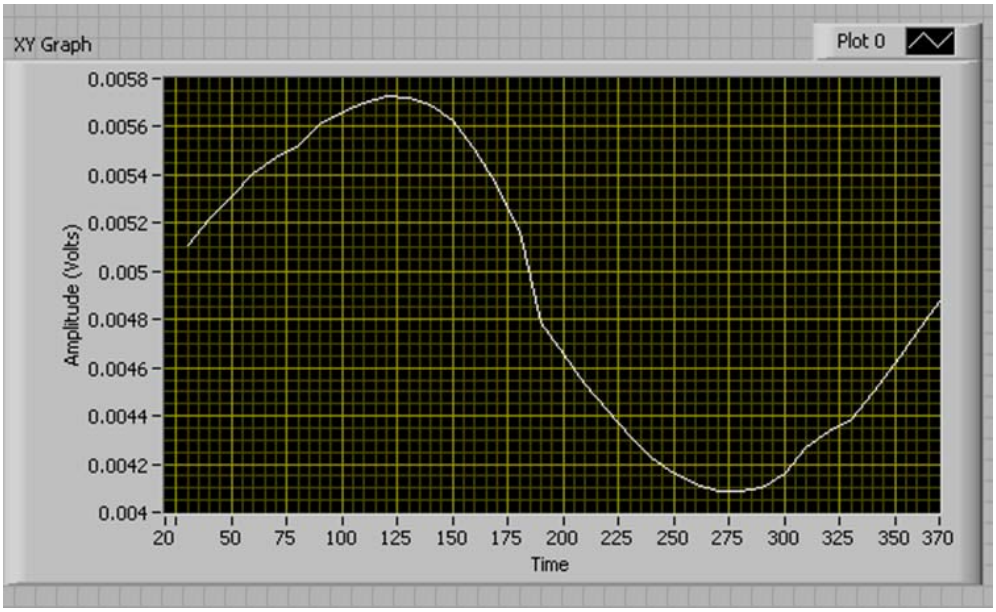

Figure 75. Measured two-way voltage using cable 3 without LPA in the circuit, "Setup II"

d. Cable 4

The measured result from "Setup I" is shown in Figure 76. The maximum is at 0 degrees. The measured two-way voltage is shown in Figure 77. The calculated one-way compensation phase using equation (13) is 310 degrees.

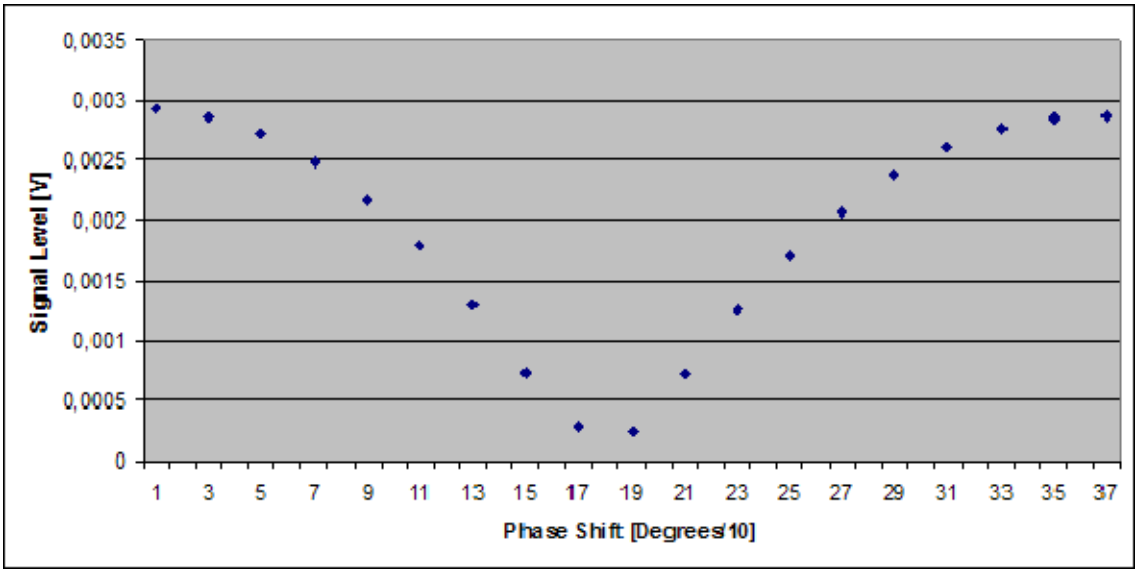

Figure 76. Measured voltage using cable 4, "Setup I"

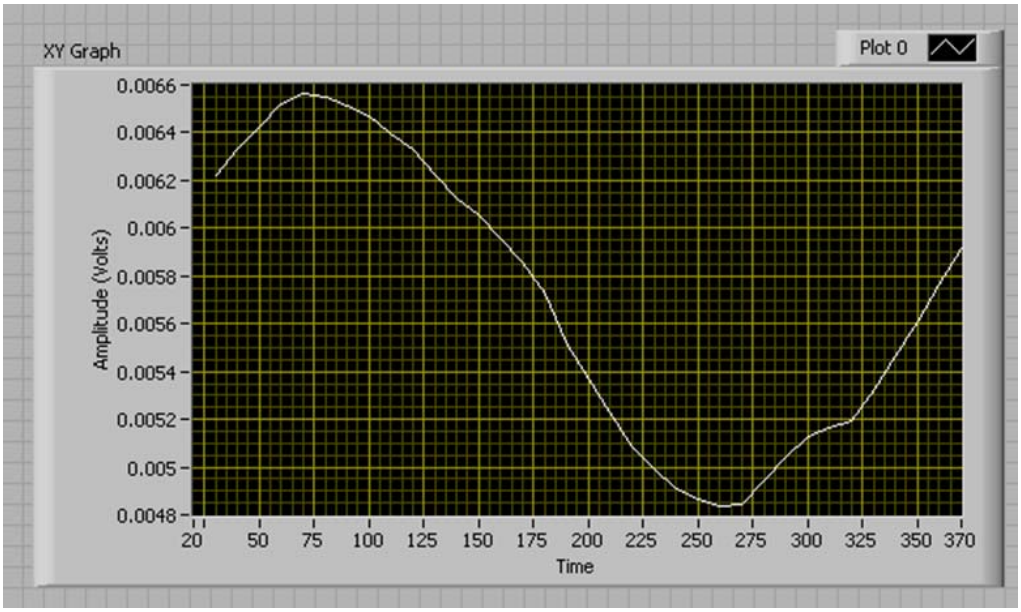

Figure 77. Measured two-way voltage using cable 4 without LPA in the circuit, "Setup II"

e. Comments on the Results

A brief summary of the data is given in Table 11. As the previous trials and their corresponding figures show, the results from the synchronization circuit are not in agreement with the expected results. Although the curves obtained by the "DDAR.lvproj" are nearly sinusoidal and have a clear minimum, they do not map to the correct phase shifts.

	Measured maximum "Setup I" [Degrees]	Calculated maximum "Setup II" [Degrees]	Error [Degrees]
Cable 1	0	305	55
Cable 2	100	240	140
Cable 3	340	320	20
Cable 4	0	310	50

Table 11. Phase for maximum voltages for "Setup I" and "Setup II"

After examination of the above results, there is not a constant value that can be added to calibrate the phase shift. Clearly there is a phase that has not been accounted for in the measurement setups. It could be an accumulation of relatively small errors from connectors and adaptors. Also, the power divider output phases were assumed equal and not measured. Finally, the modulator has some error in setting the phase, which can be as high as 5 degrees [30]. Note that measurement errors in $\Delta\phi_m$ are doubled when calculating $\Delta\phi_d$.

2. Synchronization with the LPA in the SYNC Circuit "Setup III"

In order to observe the behavior of the LPA in the synchronization circuit, the same trials were performed with the LPA included in the circuit. The schematic is shown in Figure 78.

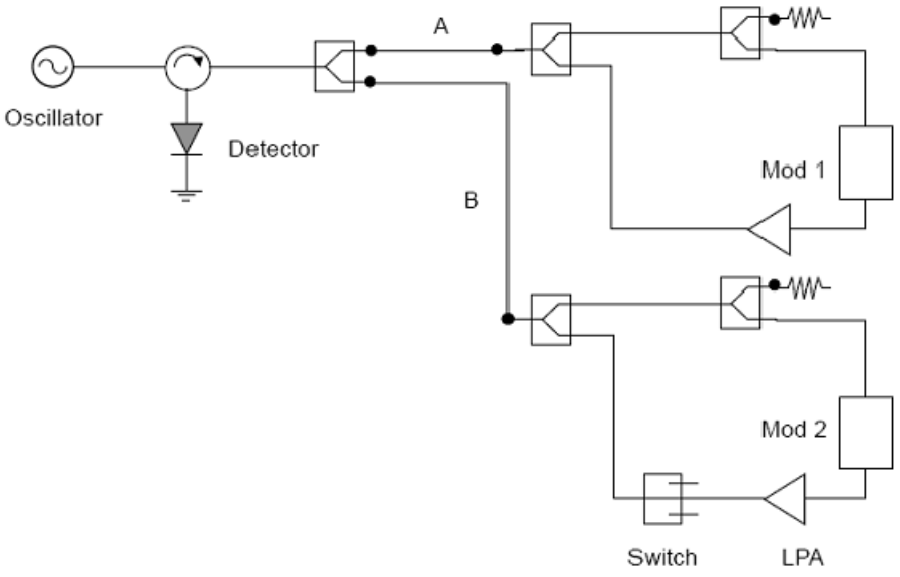

Figure 78. Setup III

a. Cable 1

As shown in the previous section (see Figure 70) the measured phase difference from "Setup I" is 0 degrees, and the measured two-way phase shift from "Setup III" is shown in Figure 79. Notice that the curve does not have a well-defined sinusoidal shape. However the spacing between the peak (~150 degrees) and the minimum (~330 degrees) is 180 degrees as expected. The calculated one-way phase is 342 degrees.

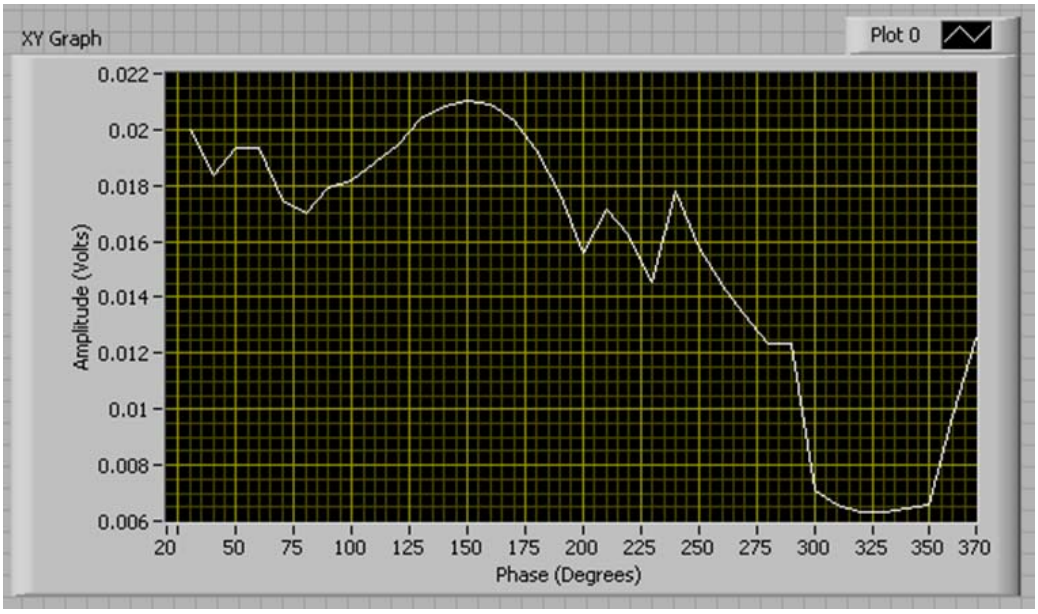

Figure 79. Measured two-way voltage using cable 1 with LPA in circuit, "Setup III"

b. Cable 2

As shown in the previous section (see Figure 72) the measured phase difference from "Setup I" is 100 degrees, and the measured two-way phase shift from "Setup III" is shown in Figure 80. The calculated one-way phase is 325 degrees.

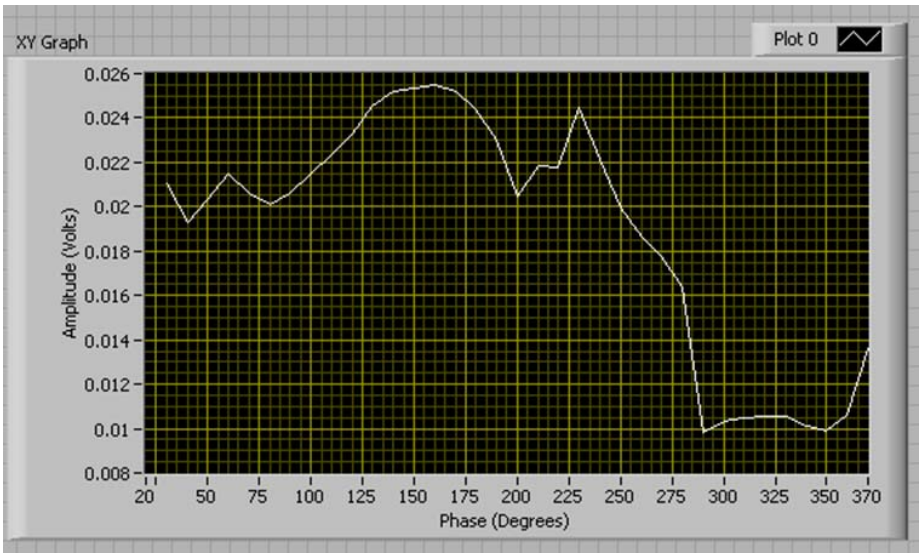

Figure 80. Measured two-way voltage using cable 2 with LPA in circuit, "Setup III"

c. Cable 3

As shown in the previous section (see Figure 74) the measured phase difference from "Setup I" is 340 degrees, and the measured two-way phase shift from "Setup III" is shown in Figure 81. The calculated one-way phase is 280 degrees.

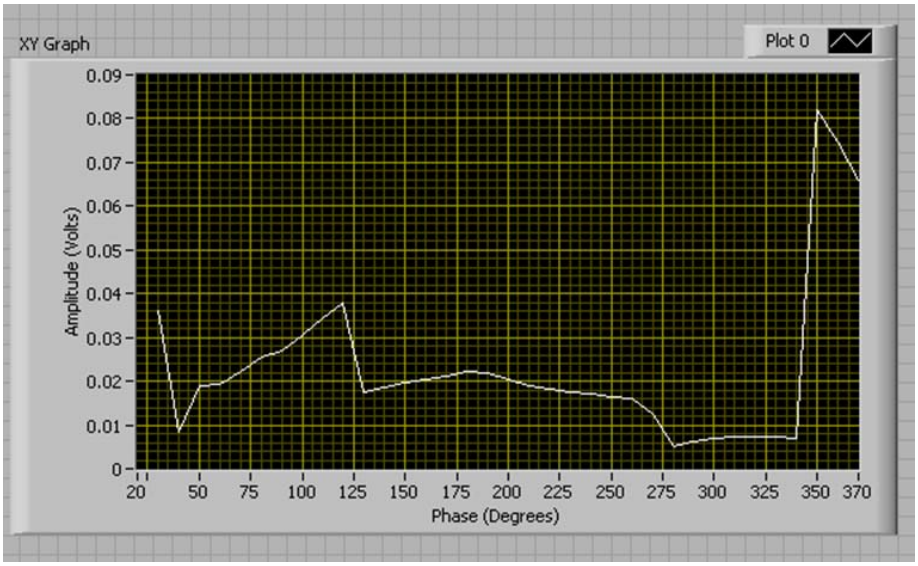

Figure 81. Measured two-way voltage using cable 3 with LPA in circuit, "Setup III"

d. Cable 4

As shown in the previous section (see Figure 76) the measured phase difference from "Setup I" is 0 degrees, and the measured two-way phase shift from "Setup III" is shown in Figure 82. The calculated one-way phase is 340 degrees.

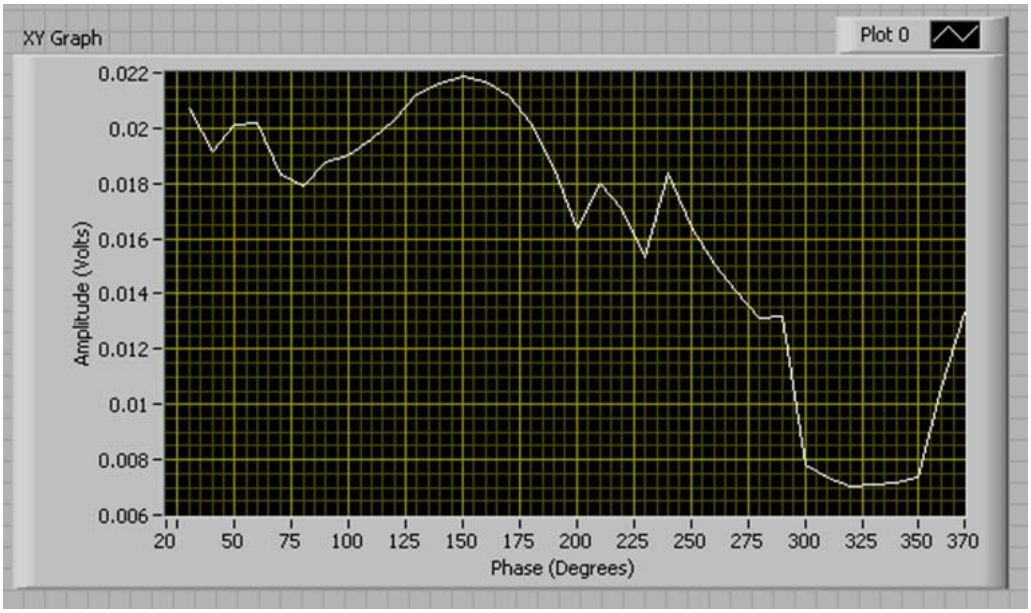

Figure 82. Measured two-way voltage using cable 4 with LPA in circuit, "Setup III"

e. Comments on the Results

In this setup the LPA is used inside the synchronization circuit, and it amplifies the transmitted signal (RFOUT) from the modulator board. Many of the curves produced by "DDAR.lvproj" do not contain any clear minimum. Furthermore, the shapes of the curves are not sinusoidal. This is likely due to leakage power levels and multiple reflections that exist in this setup. In an effort to diagnose the problem, simulations using Agilent Advanced Design System (ADS) were run. The results are presented in Section F.

E. SYNCHRONIZATION CIRCUIT WITH CIRCULATORS

In this experiment the use of a circulator instead of a splitter in the synchronization circuit is under test. Thus, a direct comparison of the two options can be presented. The details of the setup are shown in Figure 10.

1. Synchronization without the LPA in the SYNC Circuit "Setup IV"

Running the synchronization process, the resulting one-way phase shift is now 300 degrees using cable 1. "Setup IV" is essentially "Setup II" in Figure 69 with PD 1 and PD 2 replaced with circulators. (Grahn refers to this as "Setup C" [12].) The result is not significantly different than the result when synchronizing in "Setup II." The result from this demonstration is shown in Figure 83.

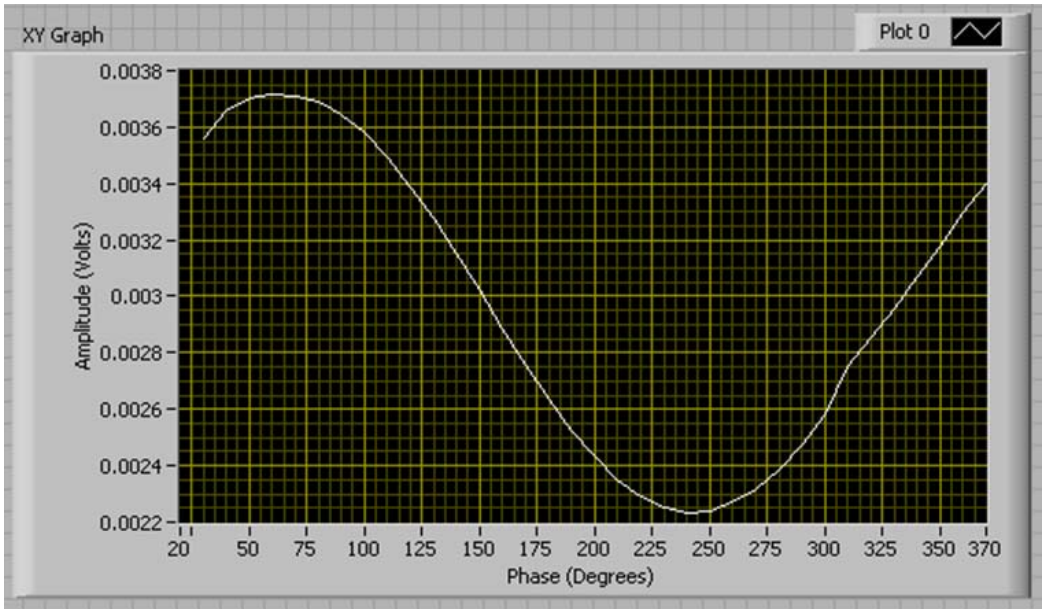

Figure 83. Measured two-way voltage using cable 1 without LPA in circuit, "Setup IV"

2. Synchronization with the LPA in the SYNC Circuit "Setup V"

The behavior of the modules when the LPA is in the circuit with a circulator is comparable with "Setup II" (see Figure 84).

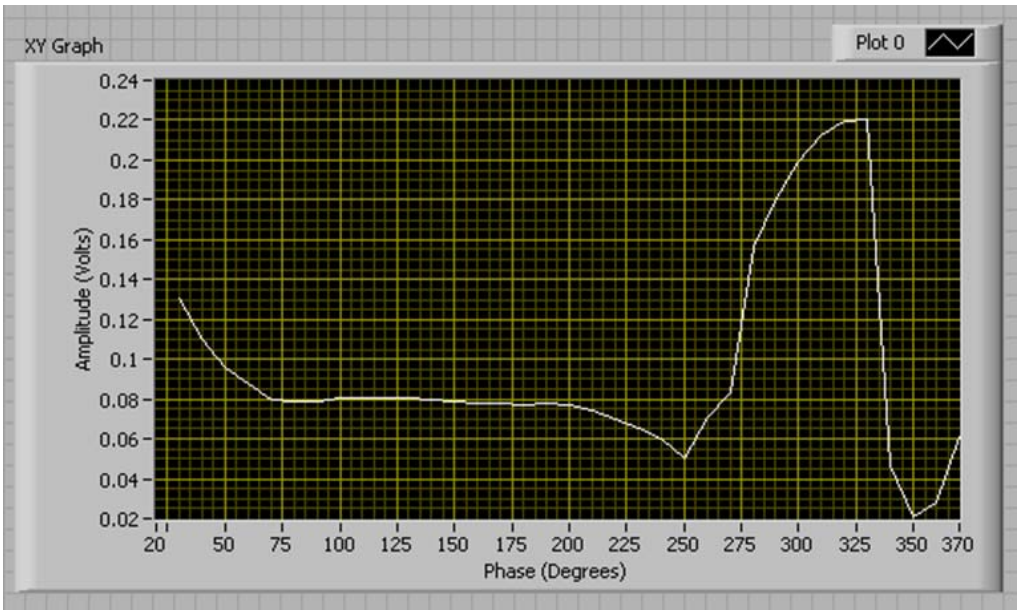

Figure 84. Measured two-way voltage using cable 1 with LPA in circuit, "Setup IV"

3. Comments on the Results

Reintroducing the circulator in the synchronization circuit did not improve the voltage curve and indicates that the "Setup II" solution is not more efficient. Furthermore, the isolation of the circulator is not a critical factor that would exclude it from being used in the synchronization circuit.

F. ADS SIMULATIONS

In order to further investigate the disagreement in the measured data, simulations of "Setup II" were performed using Agilent ADS. The schematic of "Setup II" is shown in Figure 85. In ADS the modulators are represented by a combination of an attenuator and phase shifter.

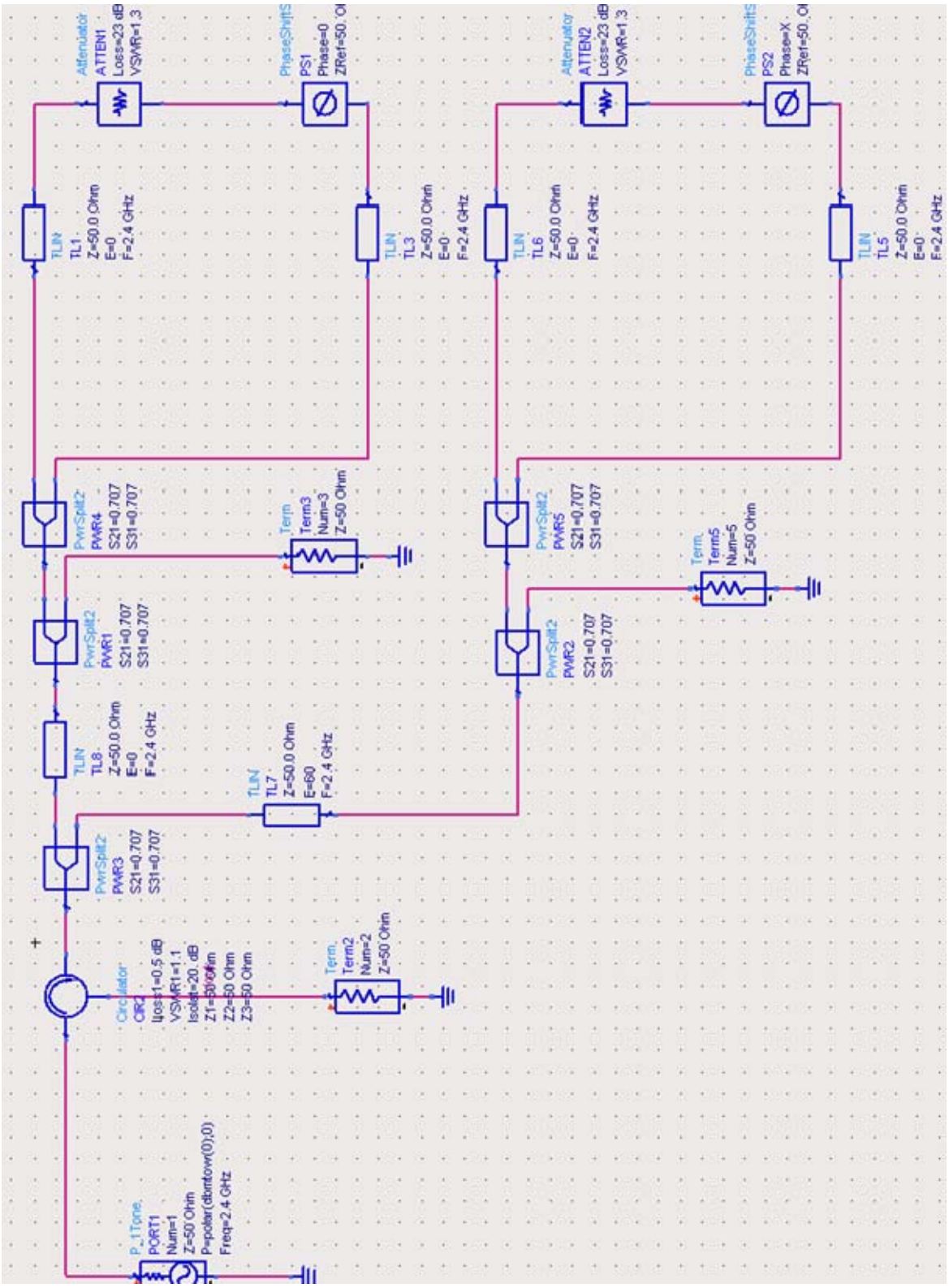

Figure 85. ADS schematic of “Setup II”

Both power dividers and circulators in “Setup II” were simulated. A 60 degree phase difference between the T/R modules was used (i.e., 60 degree phase difference between Cables A and B in Figure 69 and Figure 78). The result for ideal devices is shown in Figure 86 and the result for real devices is shown in Figure 87. These results are typical of a larger set of data that was collected.

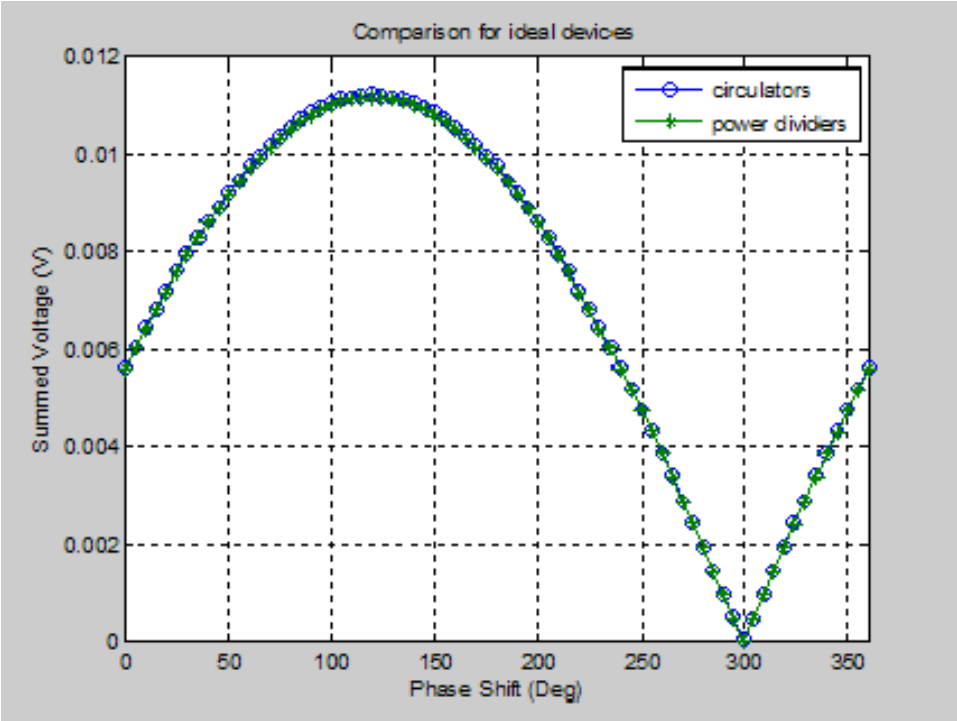

Figure 86. “Setup II” simulation results with ideal devices and 60 degrees phase difference between Cables A and B

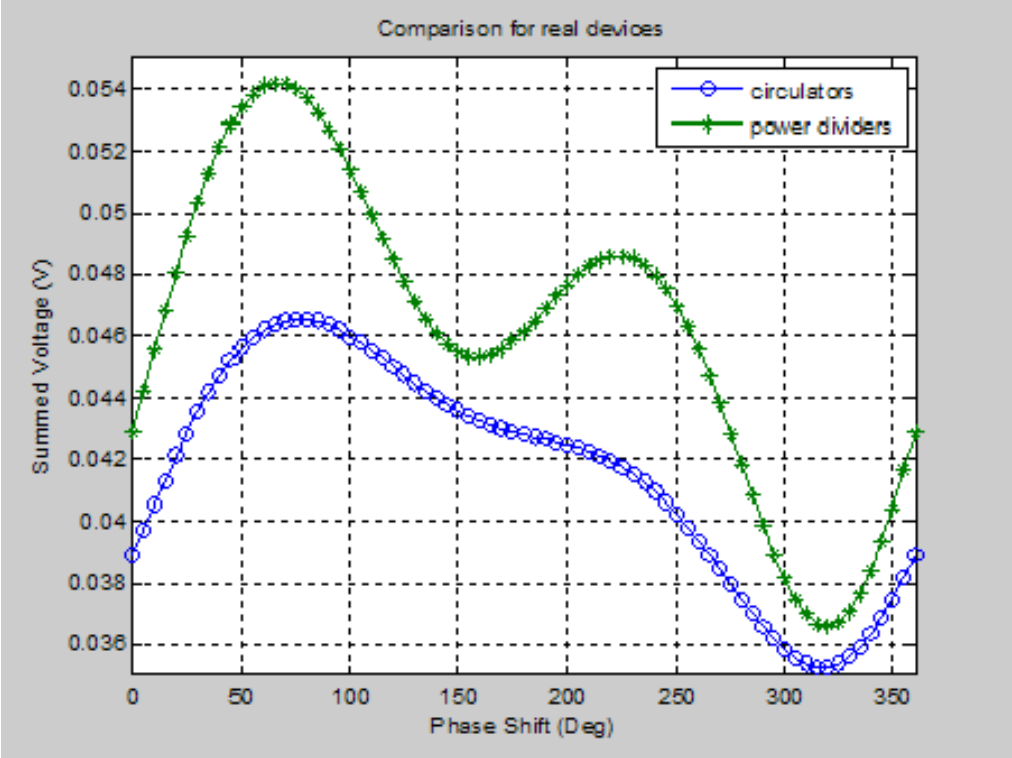

Figure 87. "Setup II" simulation results with real devices and 60 degrees phase difference between Cables A and B

The two-way result, that has the maximum located at 120 degrees, is twice the one-way result (60 degrees). These results are in agreement with equation (13). With ideal devices the results indicate that the synchronization process is theoretically correct, with zero phase error and deep nulls.

Table 12 summarizes the results from several runs. As it can be seen the real components significantly distort the results. However, the maximum and minimum locations are generally in the predicted locations.

RFOUT [dBm]		Circulator			Power divider		
		Ideal	Real	Real w/amp	Ideal	Real	Real w/amp
-14	Error [degrees]	0	5	X	0	25	X
	Notch depth [dB]	35	5	X	70	5	X
	Peak level [dBm]	-30	-23	X	-30	-22	X
-23	Error [degrees]	0	30	3	0	50	3
	Notch depth [dB]	30	2	10	70	3	7
	Peak level [dBm]	-38	-26	-19	-39	-24	-22

Notes: (a) Error is the shift in notch from expected location. (b) Notch depth is the difference between maximum and minimum voltage (i.e., constructive vs. destructive). (c) Peak level is the maximum voltage level. (d) Entries are approximate average values for phase differences from 0 to 360 degrees. (e) RFOUT is the power output from the modulation boards.

Table 12. Summary of ADS simulations

G. SUMMARY

To accomplish a demonstration of the two new T/R breadboards, five different setups were used. Initially, the power from the two modulator boards (RFOUT) was measured to find the phase shift value for a maximum using “Setup I.” Then different SYNC configurations were tested against the expected values. The two values did not agree and were of by unpredictable amounts. ADS simulations show that while the ideal case matches the theoretical values, real devices distort the results. Chapter VI presents further analysis of the data as well as conclusions and recommendations for future work.

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VI. SUMMARY, CONCLUSIONS AND RECOMMENDATIONS

A. SUMMARY AND CONCLUSIONS

The objective of this thesis was to re-examine previous thesis work and evaluate several critical aspects of the DDAR architecture. The most important task was to determine if a simple low cost synchronization circuit would perform satisfactorily. To this end two new T/R modules were built to support test and evaluation. Hardware changes can be performed in a timely and convenient fashion. Different versions of the synchronization circuit can be implemented and tested within a very limited amount of time. This modular design provided the capability to detect problems in the synchronization design, and incorporate modifications to improve performance.

Several components were redesigned or modified for that purpose. The components for the new breadboard models were evaluated from scratch, and a framework to contain both the hardware and software development was set to assist further design, development, and verification.

Also, in support of the module design, the demodulator boards have been retested to find out if use of the AGC function is feasible. After throughout analysis and measurement it was found that the dynamic range increased from 7 dB in the fixed VGIN mode to 25 dB when using the AGC. The vendor's specification states a dynamic range of 65 dB, but at an operating frequency of 2.4 GHz the dynamic range dramatically decreases. In addition, the scattering parameters of all the components of the project were measured and documented for reference. Therefore, the expected behavior of the hardware is known precisely so that measurements can be compared to simulations.

Finally new controller and processing software was developed and merged with the existing software components. All software functions are implemented in the LabVIEW project "DDAR.lvproj." It is written in a modular way which allows new functions or expanded versions of the system to be accommodated with ease. From there

all the supported functions of the system can be controlled and operated. Those include TX/RX from both the T/R modules, synchronization of the modules and generation of multiple waveforms.

The data in Chapter IV shows the measured and simulated results of phase synchronization in various configurations of the SYNC circuit.

Several configurations on the SYNC circuit were studied: with circulators, with power dividers, and with and without LNAs. Simulations with ADS showed that all configurations worked perfectly when ideal devices were used. The phase to synchronize can be determined to within a couple of degrees due to the sharp deep notches in the voltage vs. phase curve. With real device parameters, the performance is not as good due to wider notches with shallower depths. Even though, it was still possible to find the voltage minima to within 5 to 10 degrees, which is acceptable for the DDAR application.

The simulation results are not matched by the measurements. In most cases the voltage vs. phase curves are distorted and even have multiple local minima. Hence, it is impossible to calibrate the shifts with a constant phase. In all cases, the suspected problem is the leakage signals in the line between the LO and the T/R module which cause standing waves. The standing waves are very sensitive to phase shift which would explain the large changes in voltage when the module phase is changed. When the LPA is used, mismatches cause reflections that have the same magnitude as the LOIN and therefore the interference is much more pronounced.

Both the measured and simulation data indicate that this simple synchronization circuit will not perform adequately with realistic devices. The peaks and nulls of the voltage waveform are distorted and shifted, resulting in inaccurate phase compensation results.

B. RECOMMENDATIONS FOR FUTURE WORK

1. Phase Synchronization

In order to achieve accurate phase synchronization between the T/R modules, a new approach must be taken. Inserting a stable local oscillator (STALO) in each of the T/R modules is a possible option. Two configurations that utilize a STALO in every T/R module are proposed.

a. Phase Lock Loop (PLL)

The advantage of a PLL is that only a clocking signal has to be distributed from the Controller to each of the T/R modules. The phase can then be adjusted locally through the voltage controlled oscillator (VCO) that lies in every T/R module. The disadvantage is that a clocking reference must be transmitted. Also, 2.4 GHz is a very high frequency for PLL operation.

b. Demodulator Use for Phase Measurement

Another solution that embeds a STALO in the T/R module design is suggested in Figure 88. By using a demodulator board, the phase of the received reference LO signal can be measured from the I-Q data. Then it can be retransmitted by the modulator board back to the Controller and compared with the reference. The Controller assigns the compensation phase to each element's STALO signal in the processing. Therefore, the phase synchronization is completed. This is the most stable robust approach, but requires more hardware. The radar functions must be suspended during synchronization because of the switch.

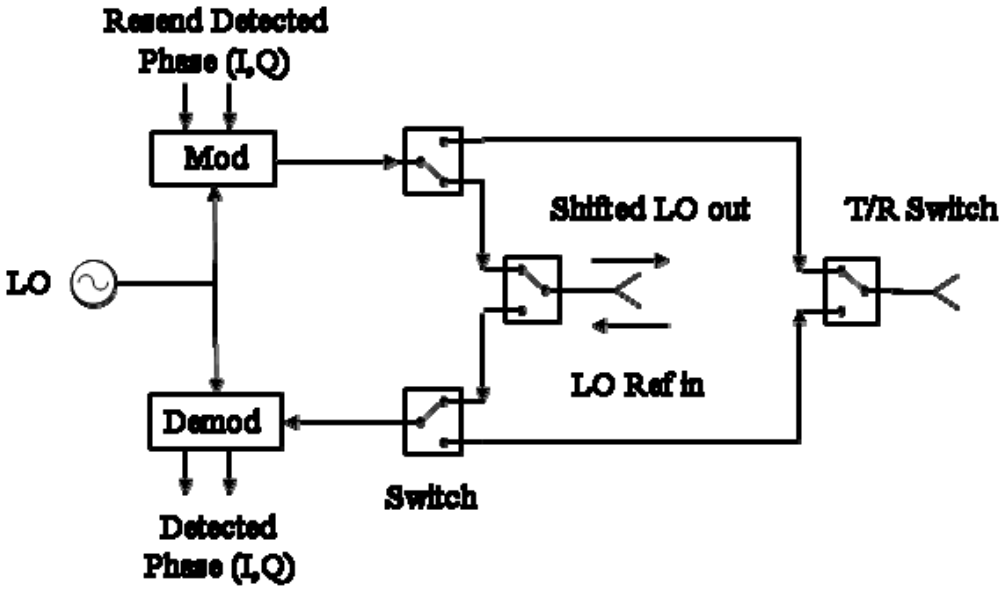

Figure 88. Demodulator use for phase measurement

c. Wireless SYNC

The proposed simple technique is not achieving the desired phase synchronization. It was tested in wired LO distribution. Once a phase synchronization solution is proved to work in the wired mode, further testing should be performed in wireless mode. Challenges include the signal levels and multipath problems.

2. Expand the Array Demonstrator

A more robust demonstration should include at least an eight-element array. Concepts such as sequential synchronization can be evaluated.

APPENDIX A. HOW TO RUN “DDAR.LVPROJ”

A. LOCATE THE PROJECT

The “DDAR.lvproj” is located on the controller computer. Log in to the “aperstructure” account and navigate to the "My Computer\djerf-tornazakis\DDAR" directory.

To open the project file manager double click on “DDAR.lvproj.” After doing that, all the VIs that the program contains are presented in a tree structure. Before proceeding, do the required hardware configuration.

B. PRELIMINARY HARDWARE CONFIGURATION

Before running the program check the following hardware configuration:

1. 5 Volts for the switches
2. 12 Volts for the LPA and LNA
3. LO – Adjust for 9 dBm to 11 dBm at the demodulator input
4. Voltmeter – ON
5. Provide power to the cRIO devices
6. Connect the cRIO controllers and the controller computer to the LAN

C. RUNNING “DDAR.LVPROJ”

Expand the Main folder on the tree structure so the “Main_2.vi” is visible. Double click on “Main_2.vi” to start the program. To run “Main_2.vi” you have to click on the run arrow on the LabVIEW toolbar. Once the program is running you can operate the two main menus, namely NORM and SYNC.

To activate each of the modes you have to select the desired menu from the dropdown list and then press the green button next to it that says “Activate Menu.”

The screen space is partitioned in two grouped areas corresponding to the menus. When the "Activate Menu" button is pressed one can notice that the green LED of the selected menu is turned ON. This provides a visual aid as to which menu is currently active. Their position is highlighted in Figure 89.

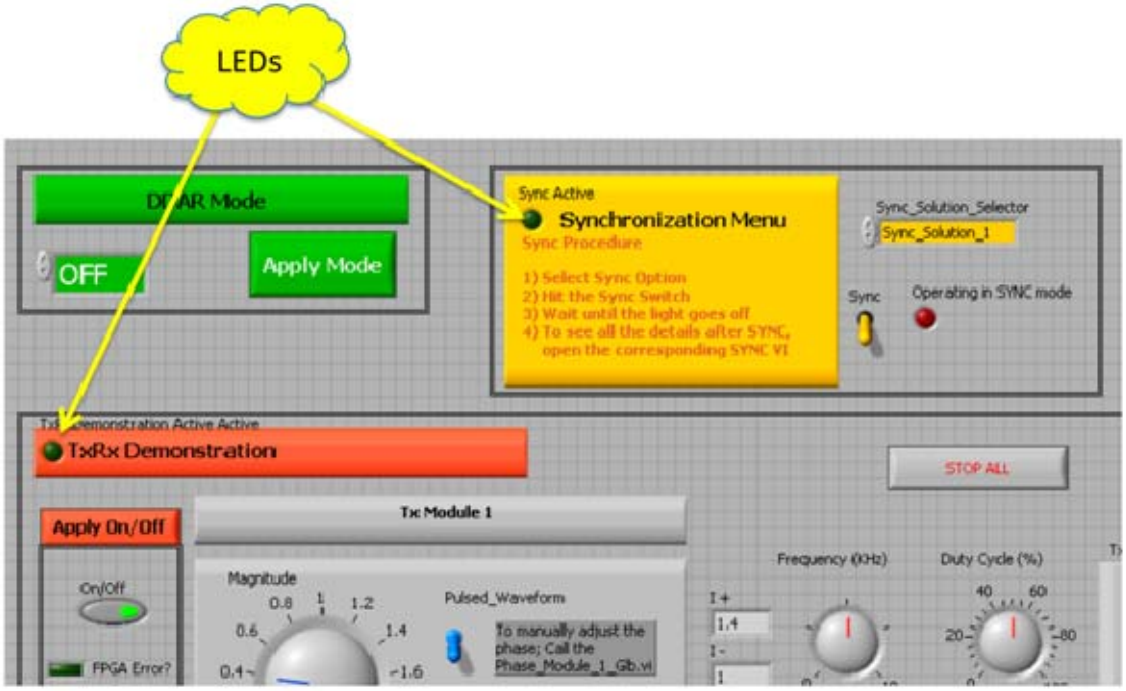

Figure 89. LEDs to indicate which block is active

1. SYNC Menu

Once the SYNC menu is selected and the "Activate Menu" button is pressed, the green LED next to the SYNC menu banner is turned ON. Now one can select the Sync option 1 or 2 and then hit the SYNC switch to allow the synchronization process to execute. Upon completion, the SYNC process terminates automatically, the LED on the banner turns OFF and control is returned back to the menu choice area. Notice that at this moment, the phase on the global variable for the module 2 is set. However, if one examines the TX part of module 2 below on the GUI it will still show zero for phase 2. This is because the NORM mode needs to be executed so the global variable of the phase 2 is read to the "Main_2.vi."

2. NORM Menu

After selecting the NORM menu and pressing the green "Activate Menu" button next to it, the LED next to the NORM mode banner is set to ON. Now the user can select what module functions to observe. The ON/OFF buttons on the left hand part of the NORM menu can be used to select which module the user want to set in TX or RX mode. Once those buttons are set, the red button named "Apply On/Off" should be pressed to allow the mode to continue its execution. At this point the actual values on the I and Q graphs will be updated continuously. Furthermore, any phase changes that were done in the SYNC program will take effect. To abort individual channels the user can hit the corresponding STOP buttons. To abort the NORM mode, the user needs to press the "STOP ALL" button that is in the middle-top of the NORM mode area. Notice that the "STOP ALL" button should be pressed for a second time to be reset for the next use. One should not forget this step. The NORM mode termination is confirmed by the extinction of the LED next to the banner and control is returned to the menu selection area. The sequence of user selections inside the NORM mode is shown in Figure 90.

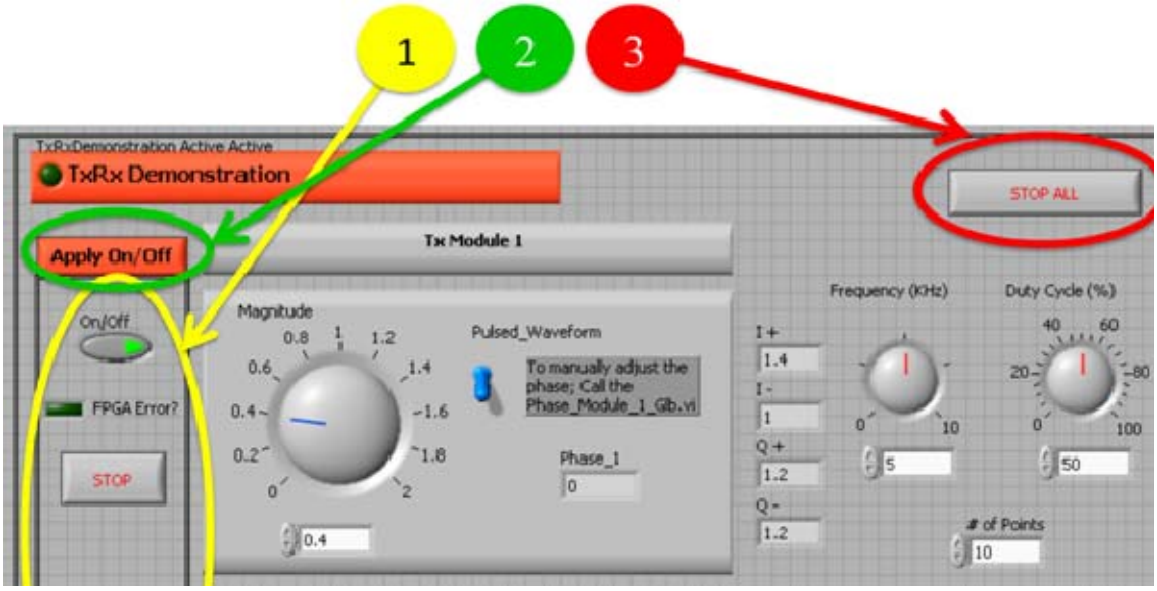

Figure 90. Sequence of user selections in NORM mode

D. EXITING “DDAR.LVPROJ”

Terminating the program from the stop button on the LabVIEW toolbar is equivalent to killing its processes. This forces the program to terminate without performing its exiting operations. Unsaved data or other inconsistencies may arise. Instead, one should use the normal termination procedure as follows.

Once the user exits the current mode of operation and the control returns to the menu selection, the OFF option should be selected from the drop down menu. Then, once the green “Activate Mode” switch is hit, “Main_2.vi” will terminate normally.

APPENDIX B. SCATTERING PARAMETERS

In this appendix, all the scattering parameters data of the components used for the construction of the additional two T/R-modules are shown. They are provided for reference and further investigation if needed. Splitter data is shown in Figures 91 through 122, switch data in Figures 123 through 158, LNA data in Figures 159 through 166, LPA data in Figures 167 through 174.

A. SPLITTER 1

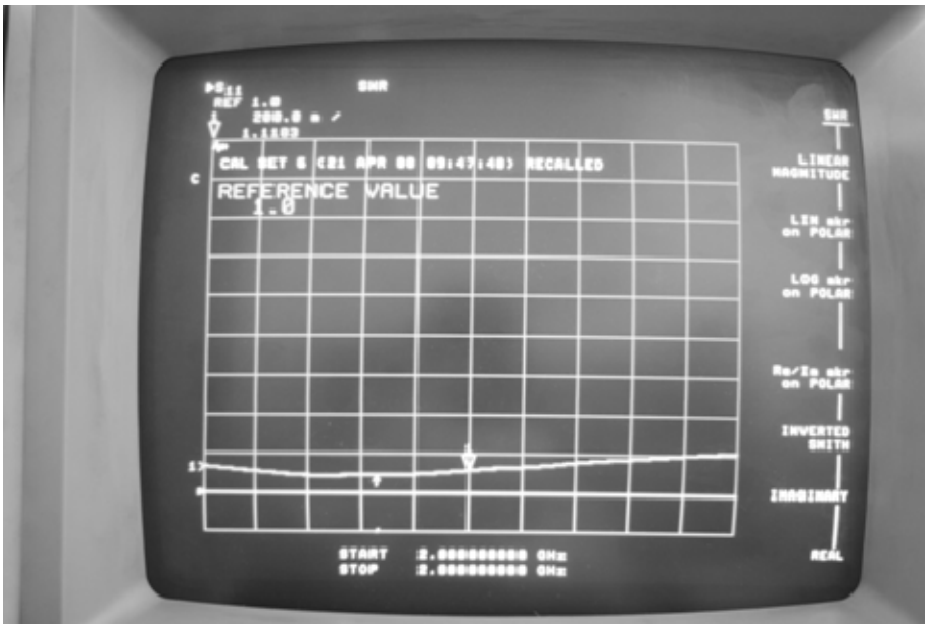

Figure 91. Splitter1; Port 1; S11

Figure 92. Splitter1; Port1; S22

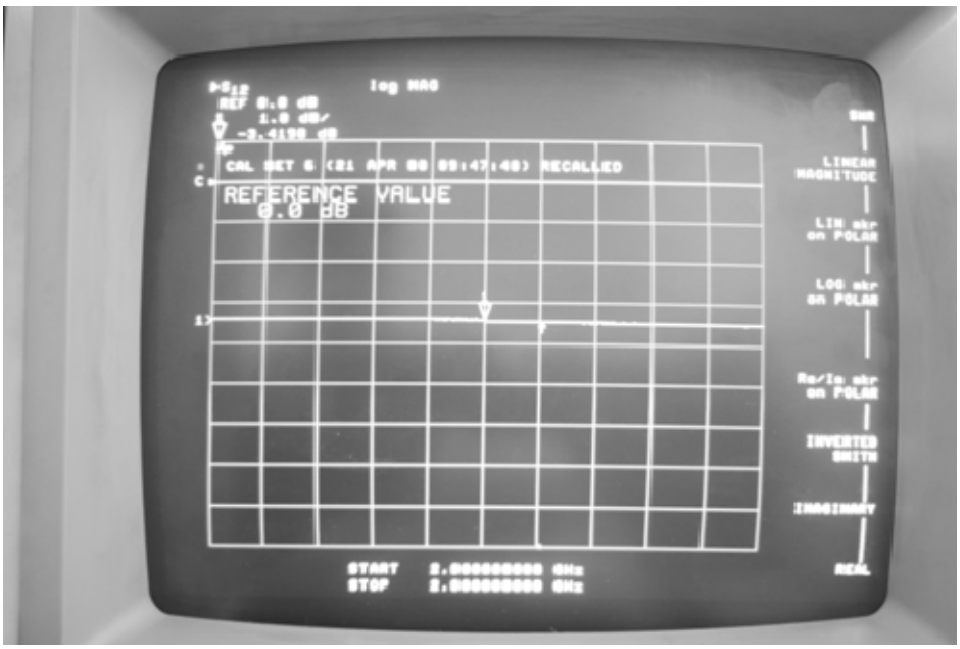

Figure 93. Splitter1; Port1; S12

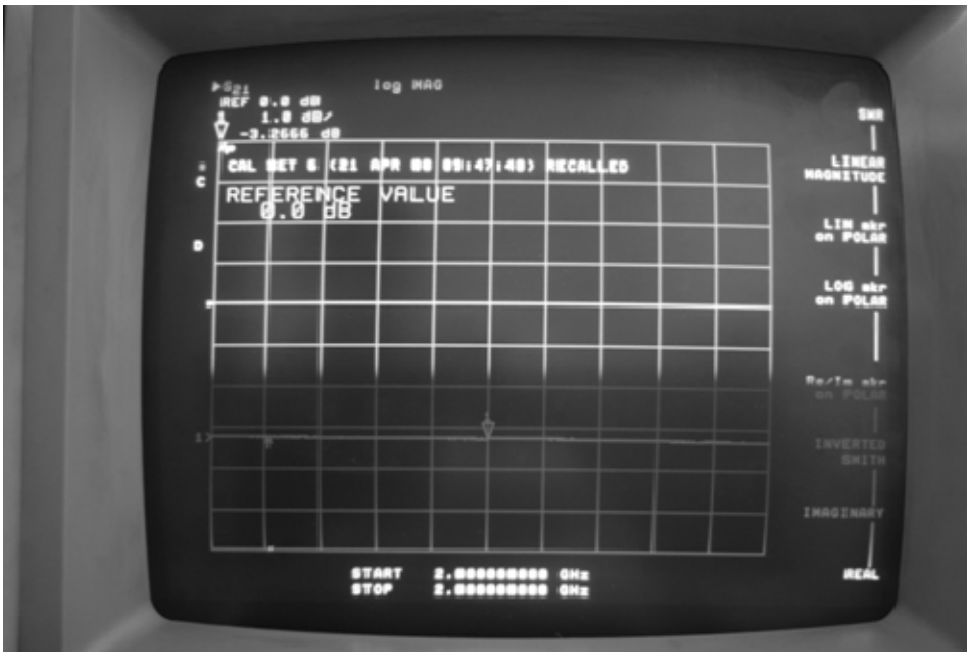

Figure 94. Splitter1; Port1; S21

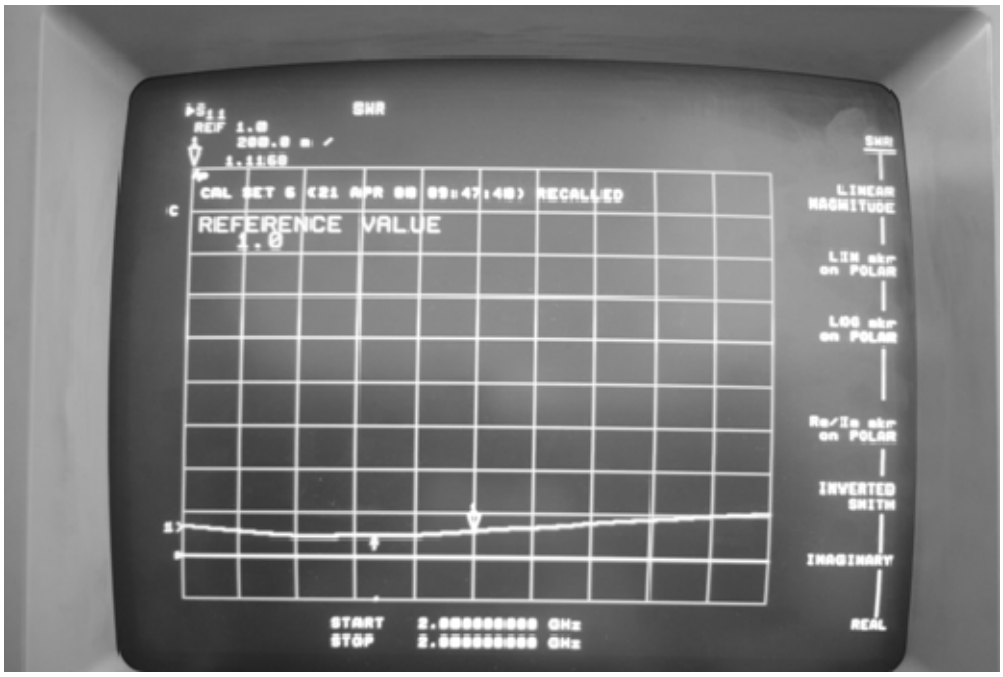

Figure 95. Splitter1; Port2; S11

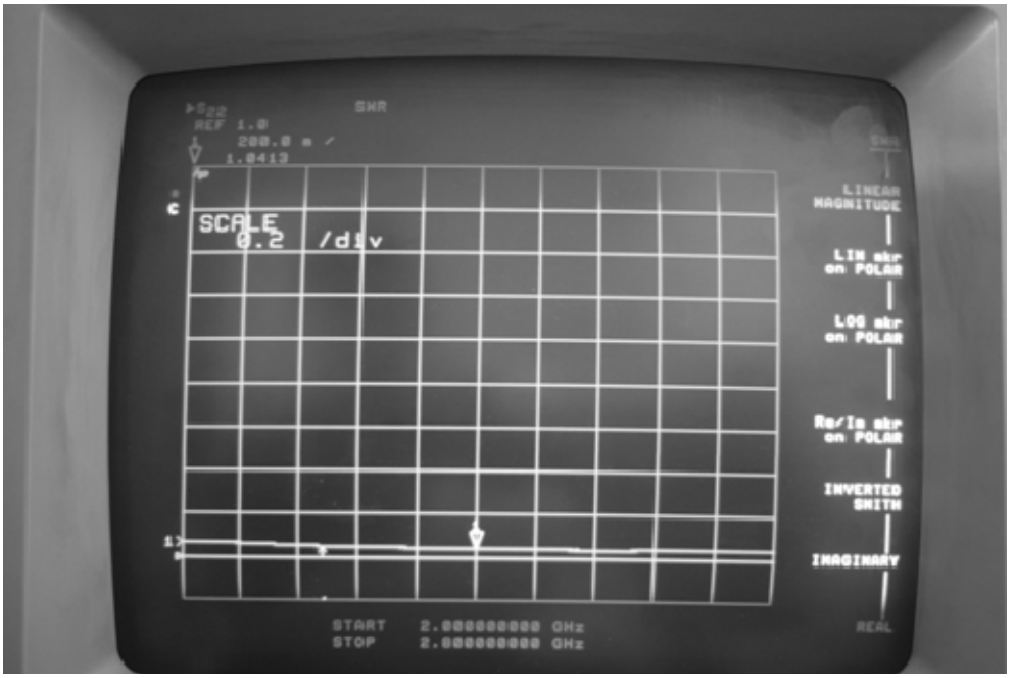

Figure 96. Splitter1; Port2; S22

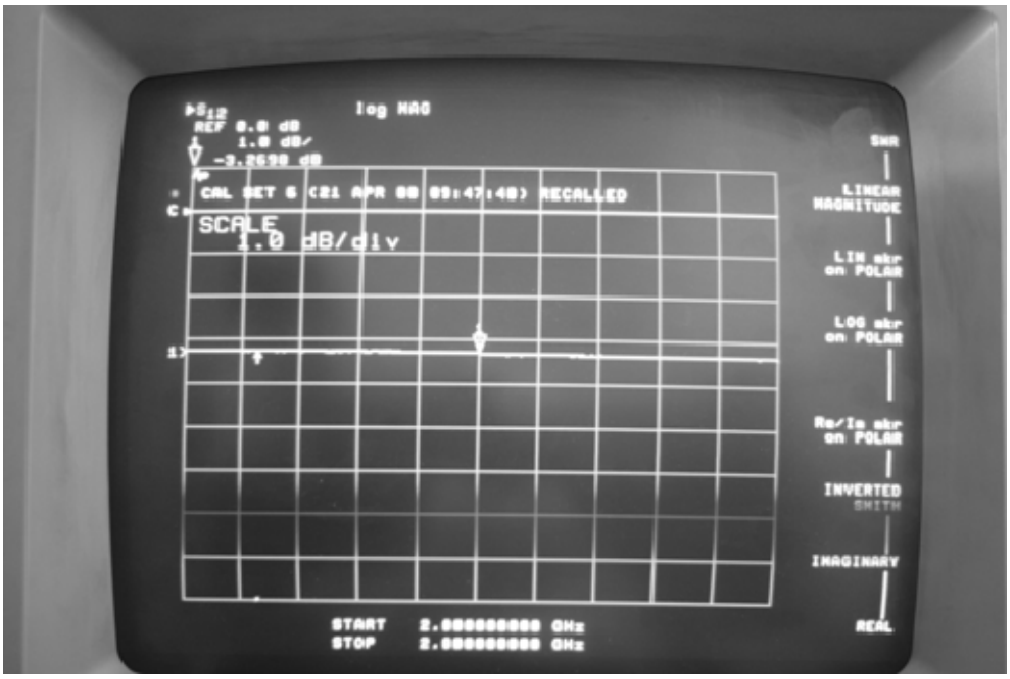

Figure 97. Splitter1; Port2; S12

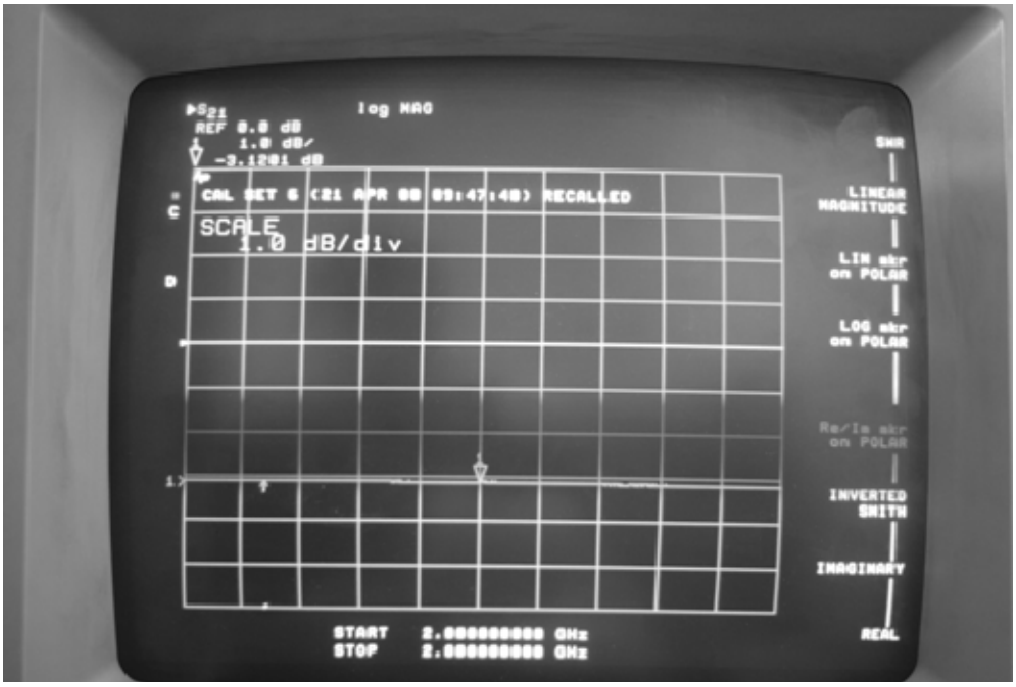

Figure 98. Splitter1; Port2; S21

B. SPLITTER 2

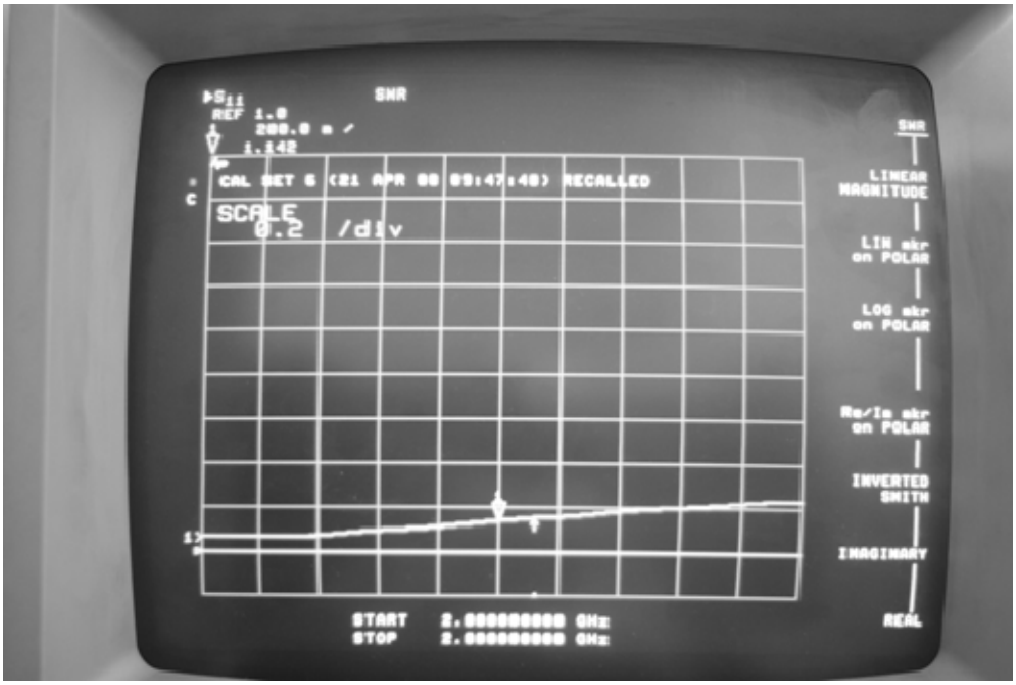

Figure 99. Splitter2; Port1; S11

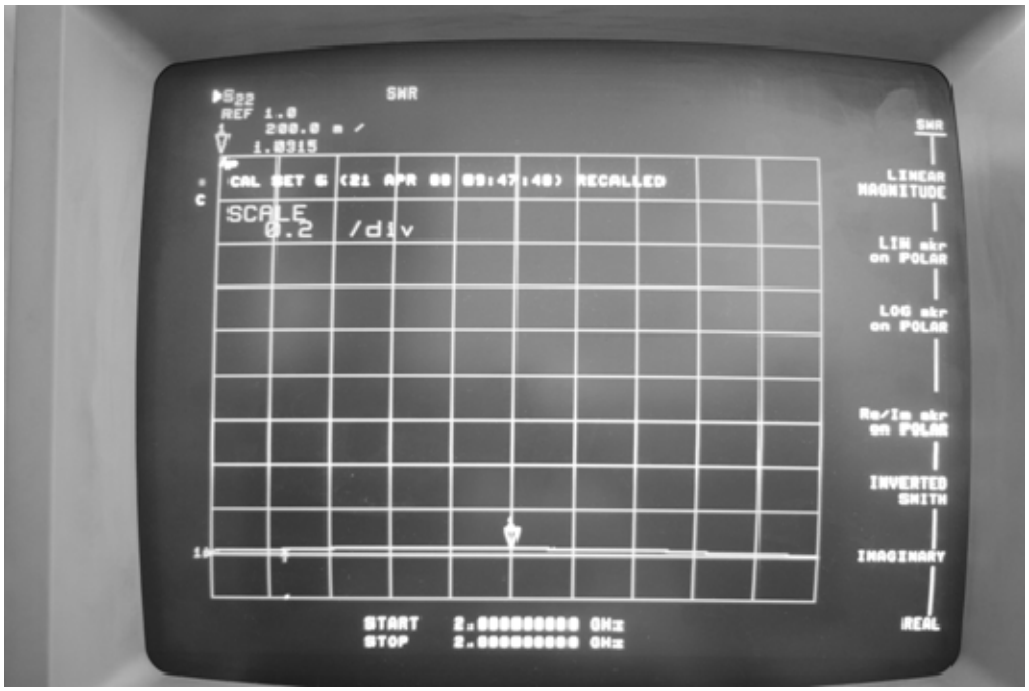

Figure 100. Splitter2; Port1; S22

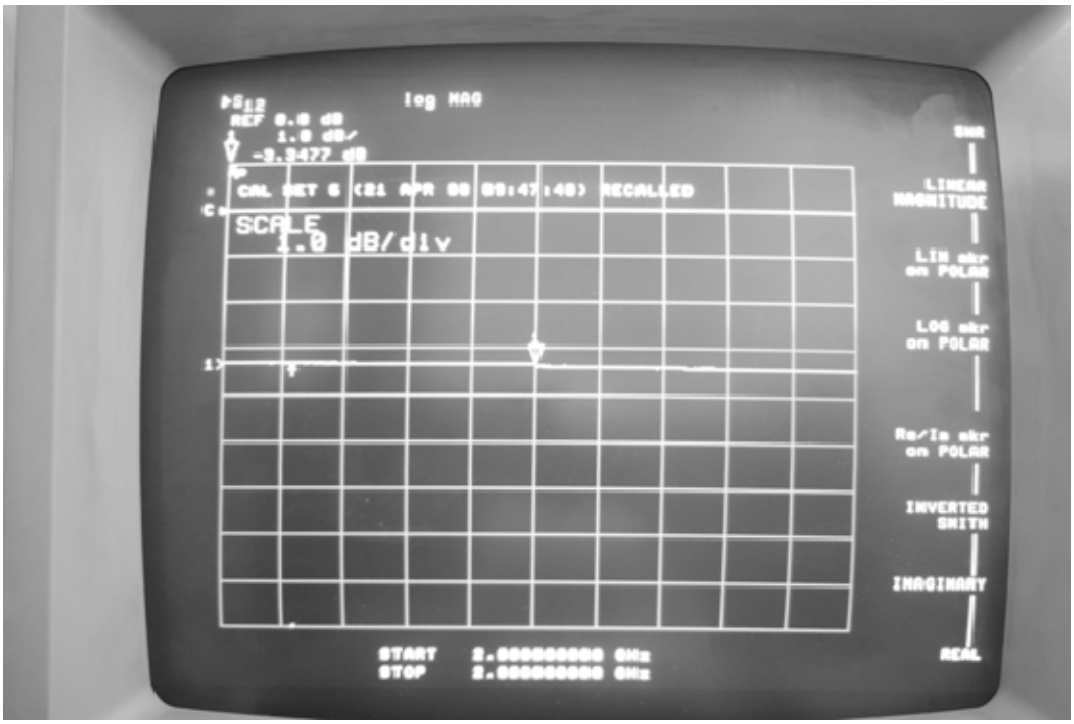

Figure 101. Splitter2; Port1; S12

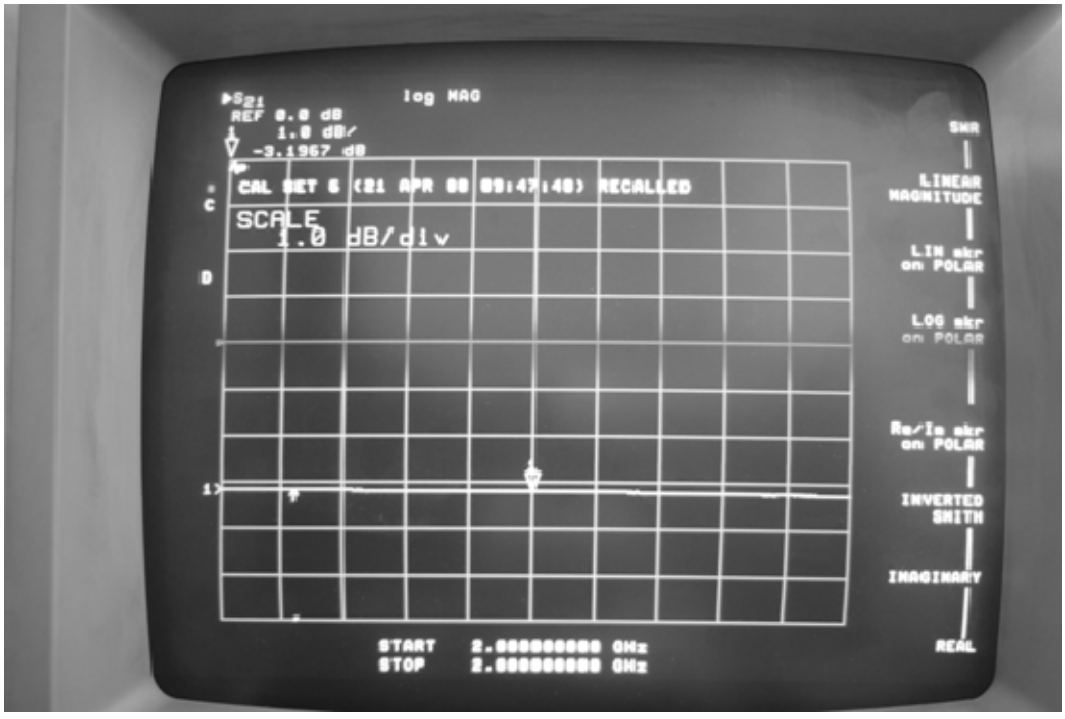

Figure 102. Splitter2; Port1; S21

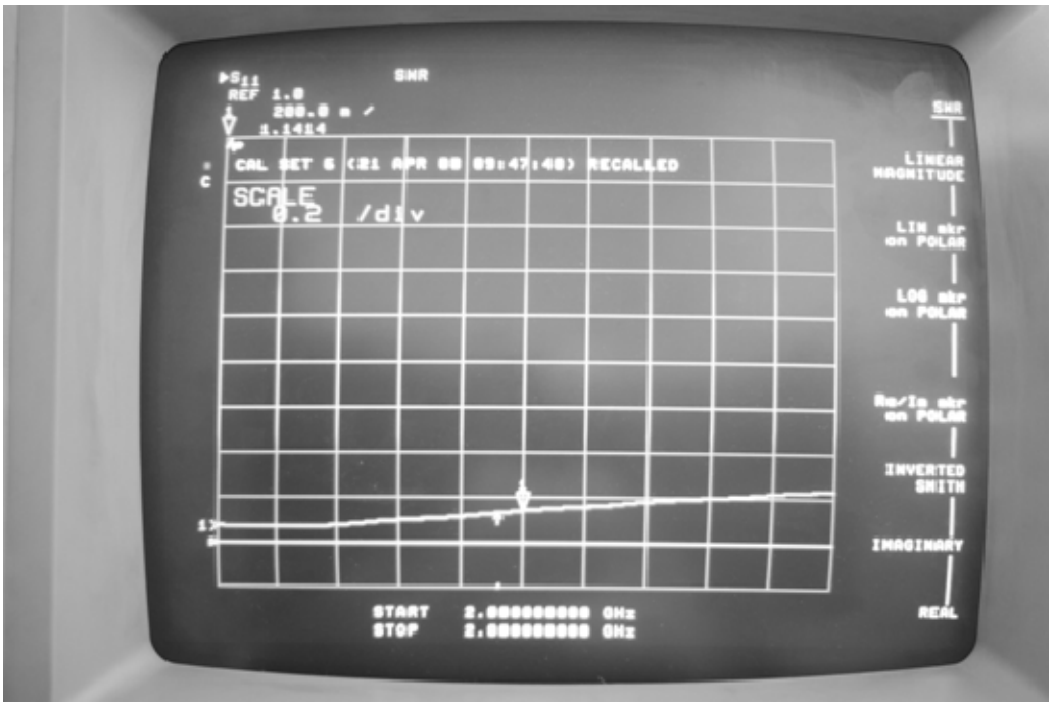

Figure 103. Splitter2; Port2; S11

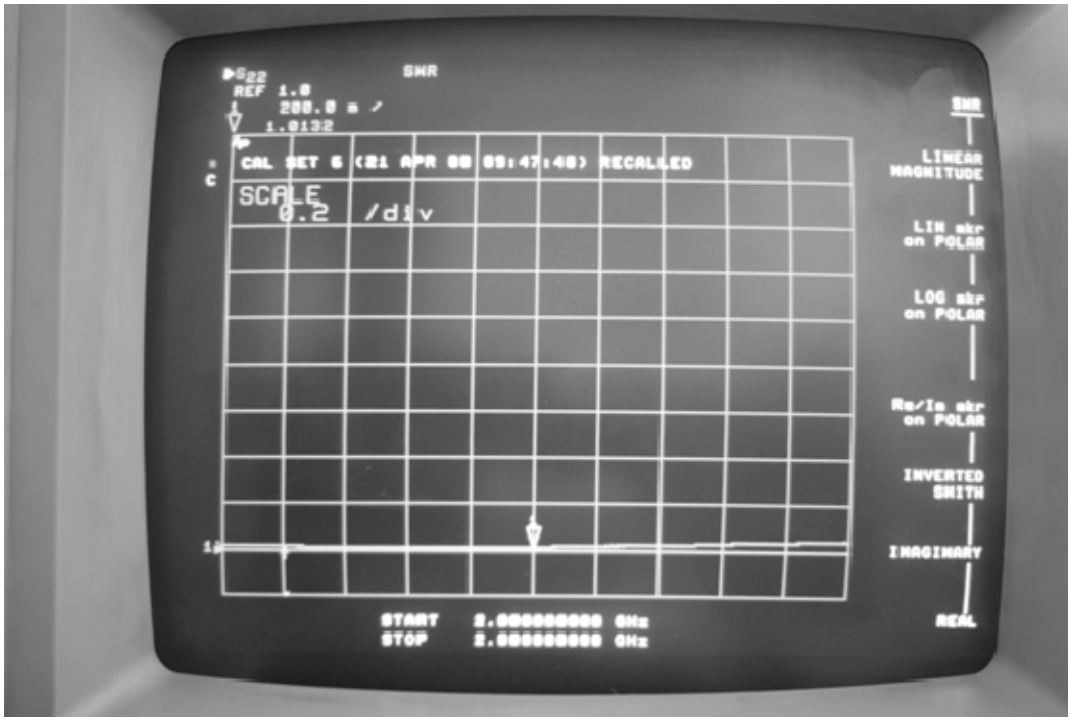

Figure 104. Splitter2; Port2; S22

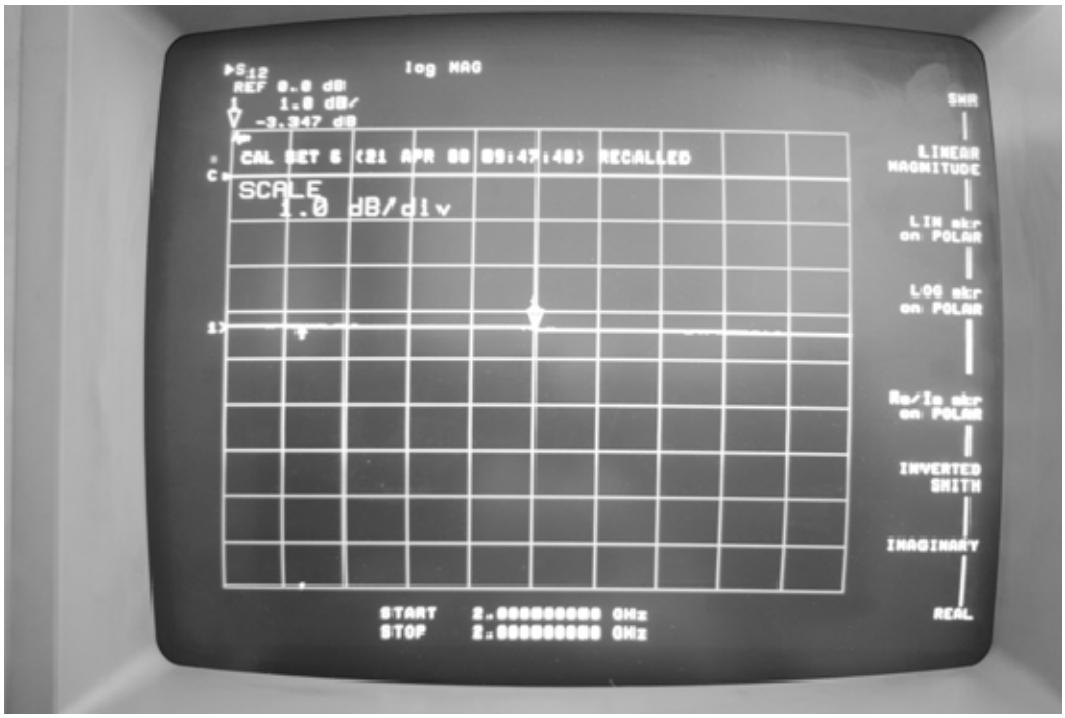

Figure 105. Splitter2; Port2; S12

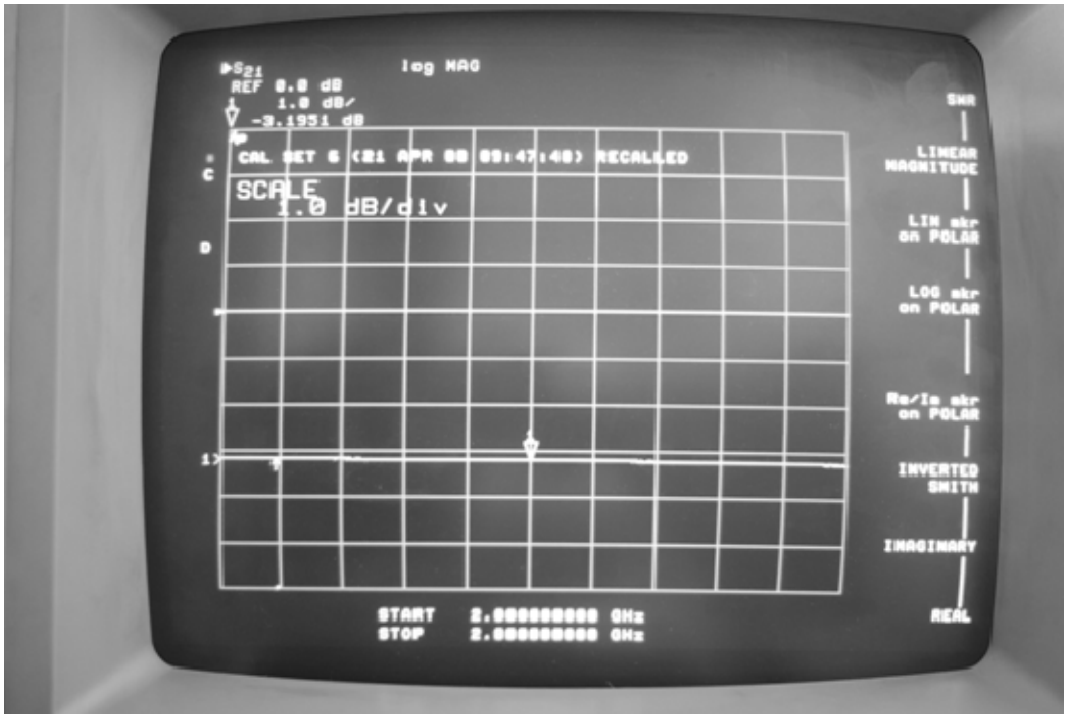

Figure 106. Splitter2; Port2; S21

C. SPLITTER 3

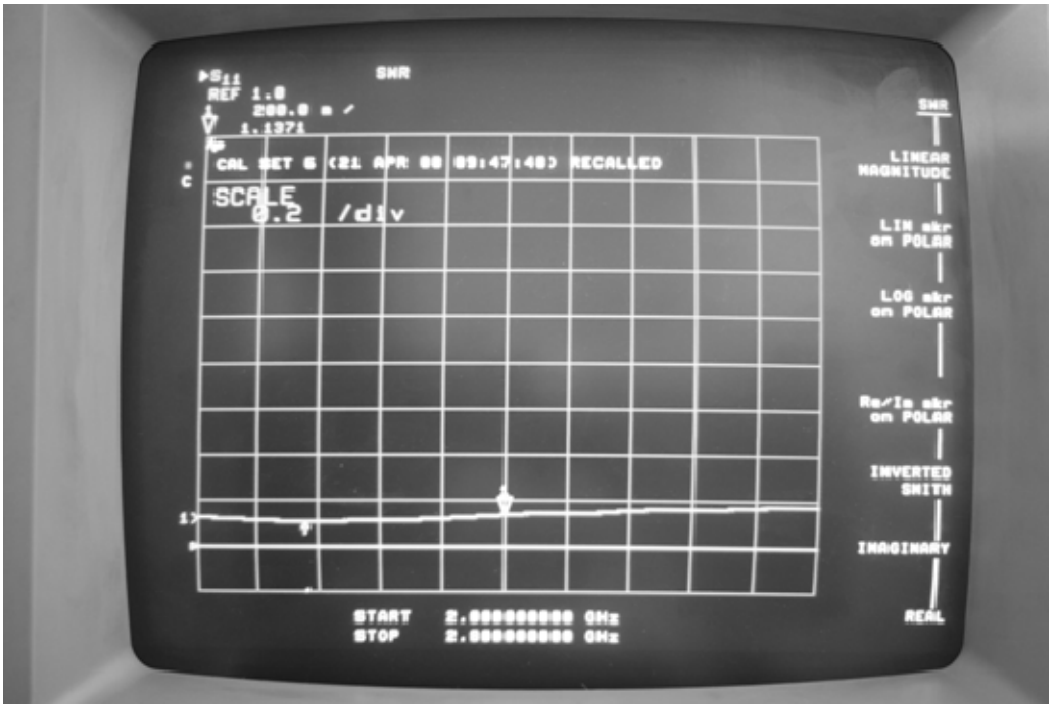

Figure 107. Splitter3; Port1; S11

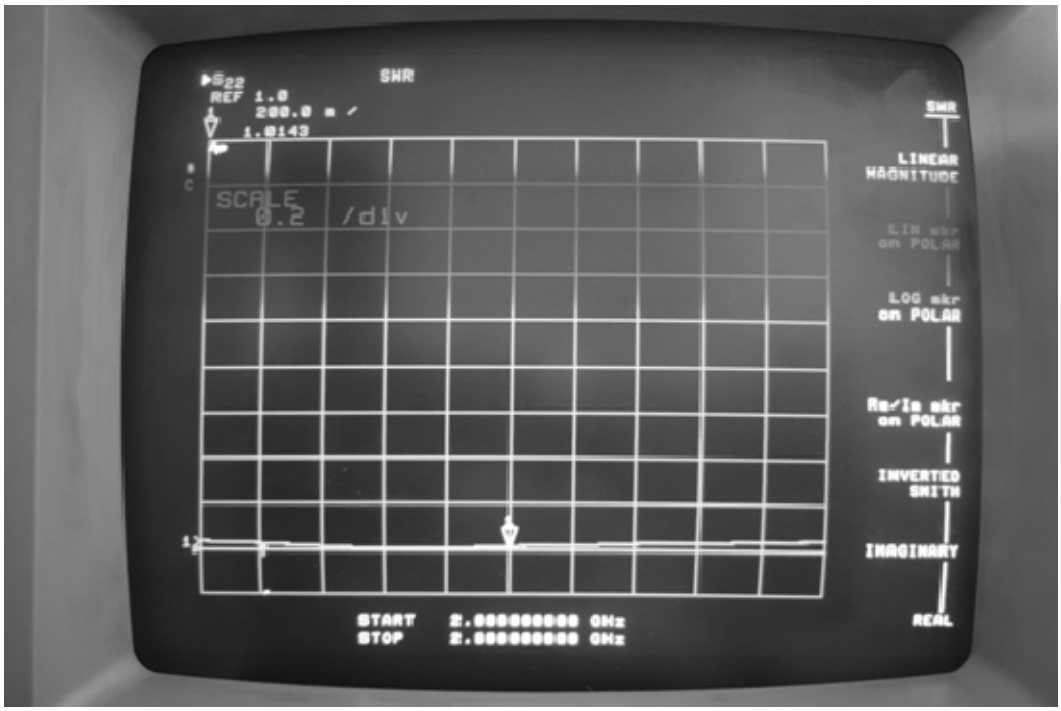

Figure 108. Splitter3; Port1; S22

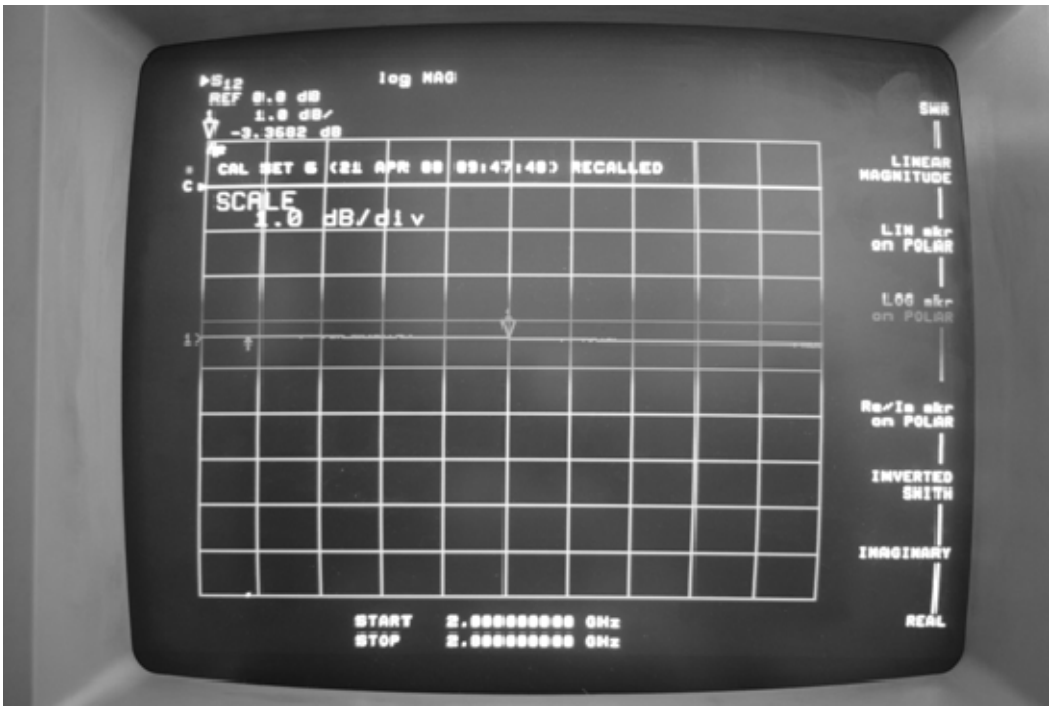

Figure 109. Splitter3; Port1; S12

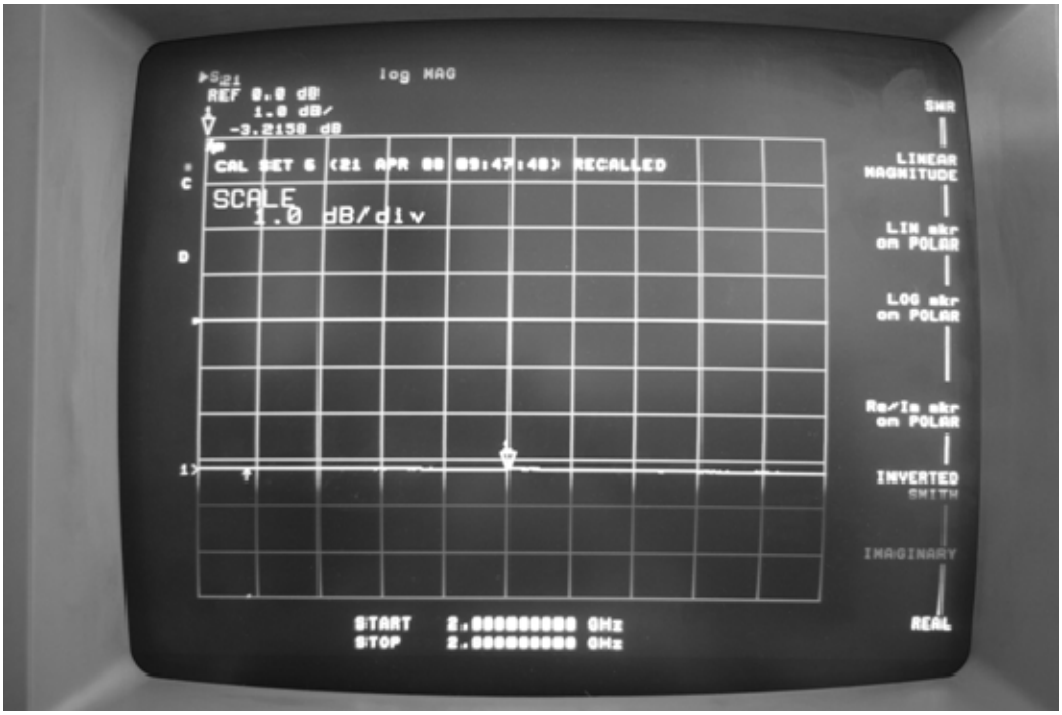

Figure 110. Splitter3; Port1; S21

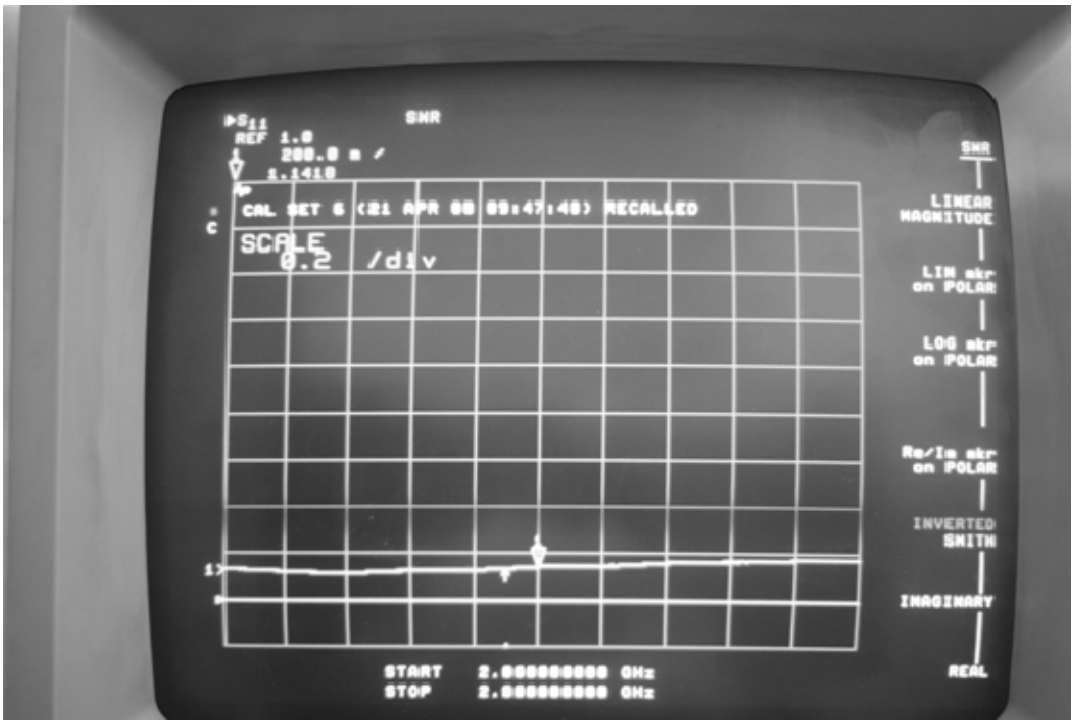

Figure 111. Splitter3; Port2; S11

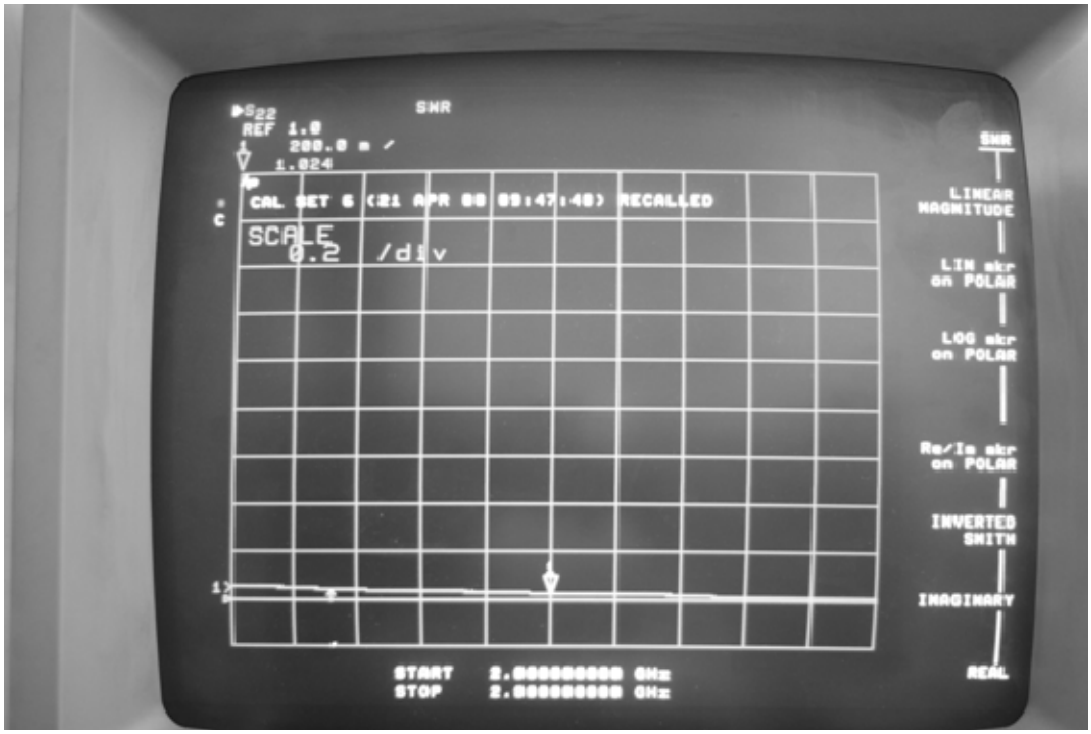

Figure 112. Splitter3; Port2; S22

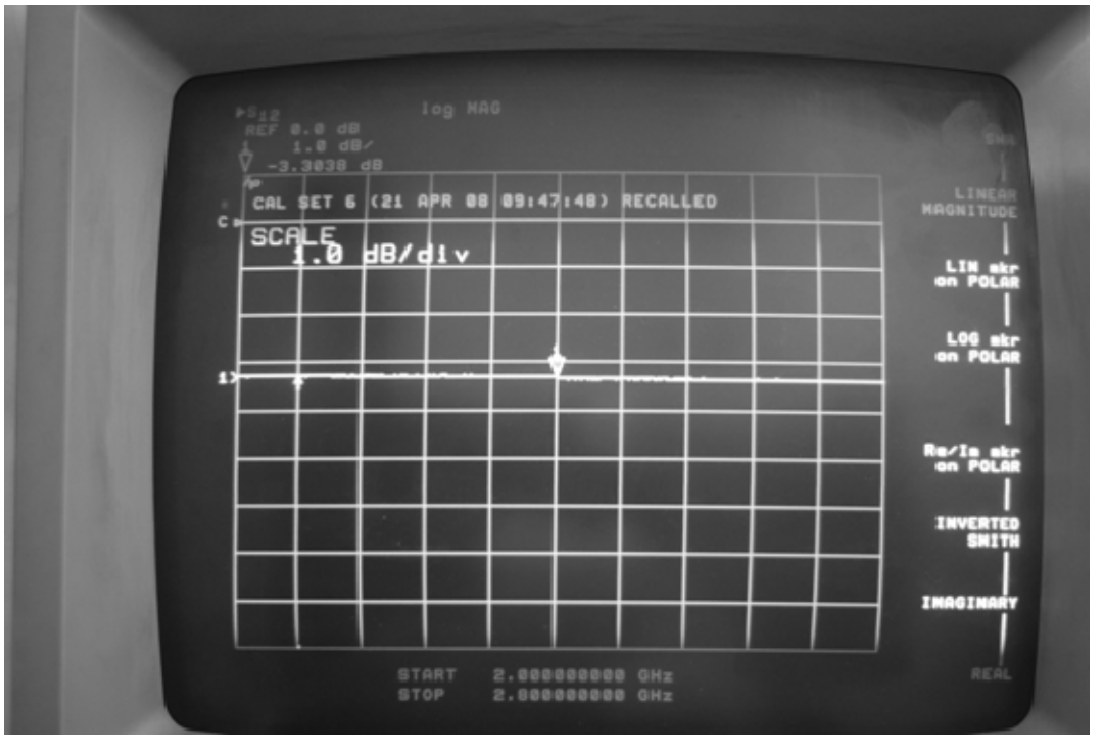

Figure 113. Splitter3; Port2; S12

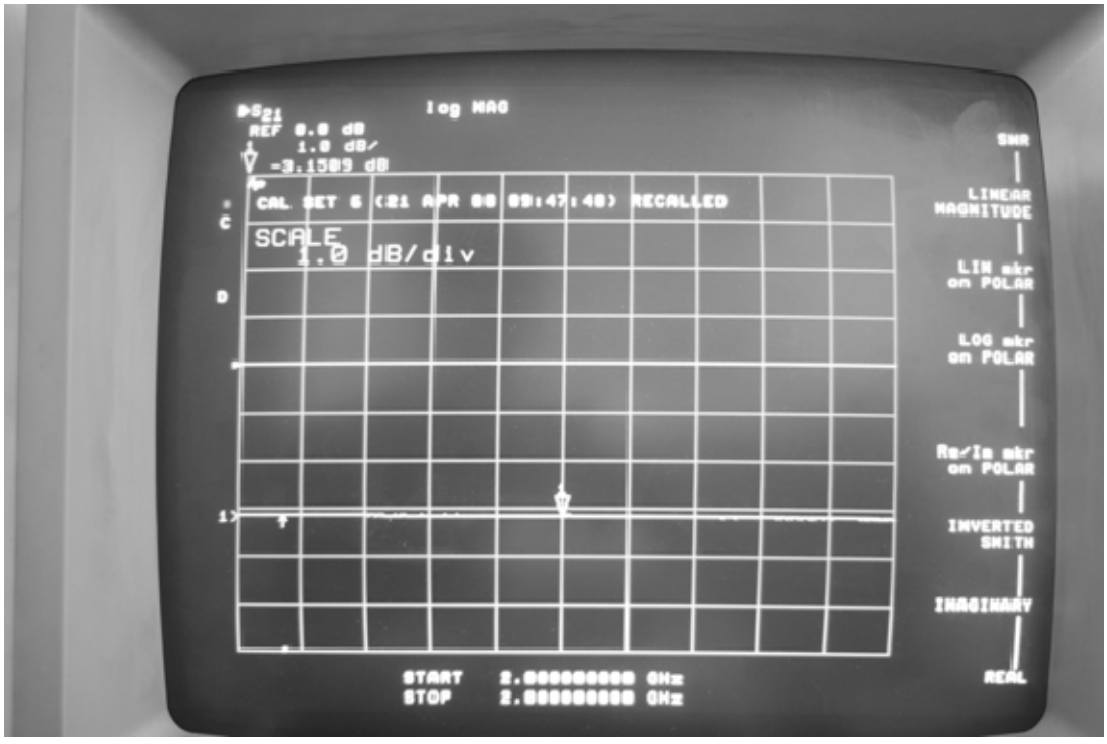

Figure 114. Splitter3; Port2; S21

D. SPLITTER 4

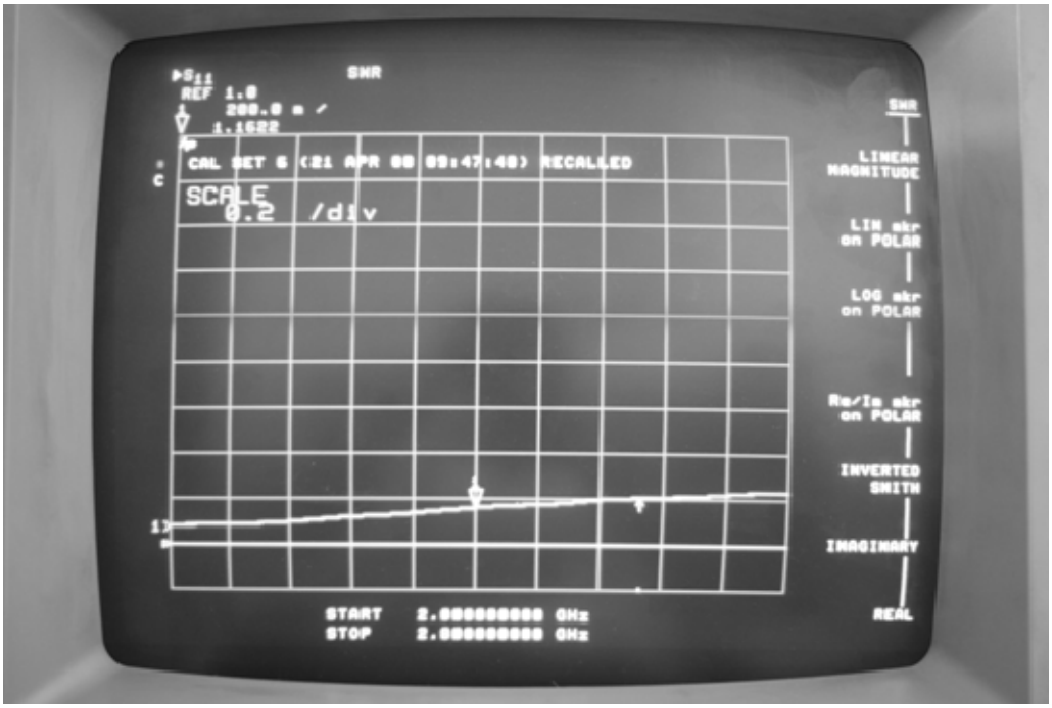

Figure 115. Splitter4; Port1; S11

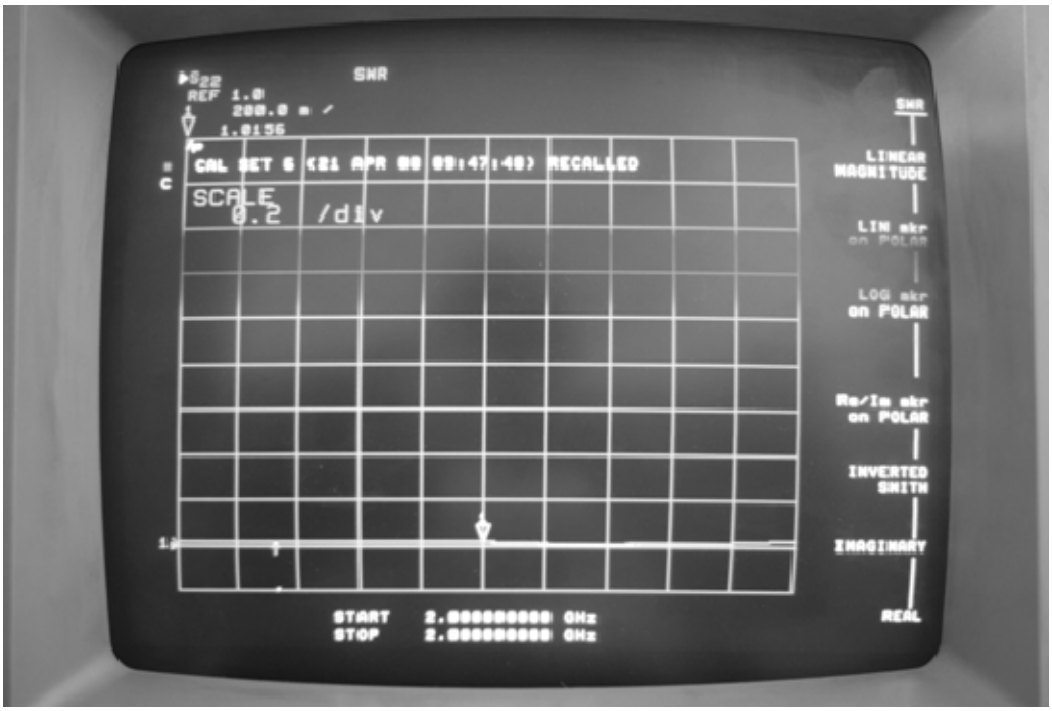

Figure 116. Splitter4; Port1; S22

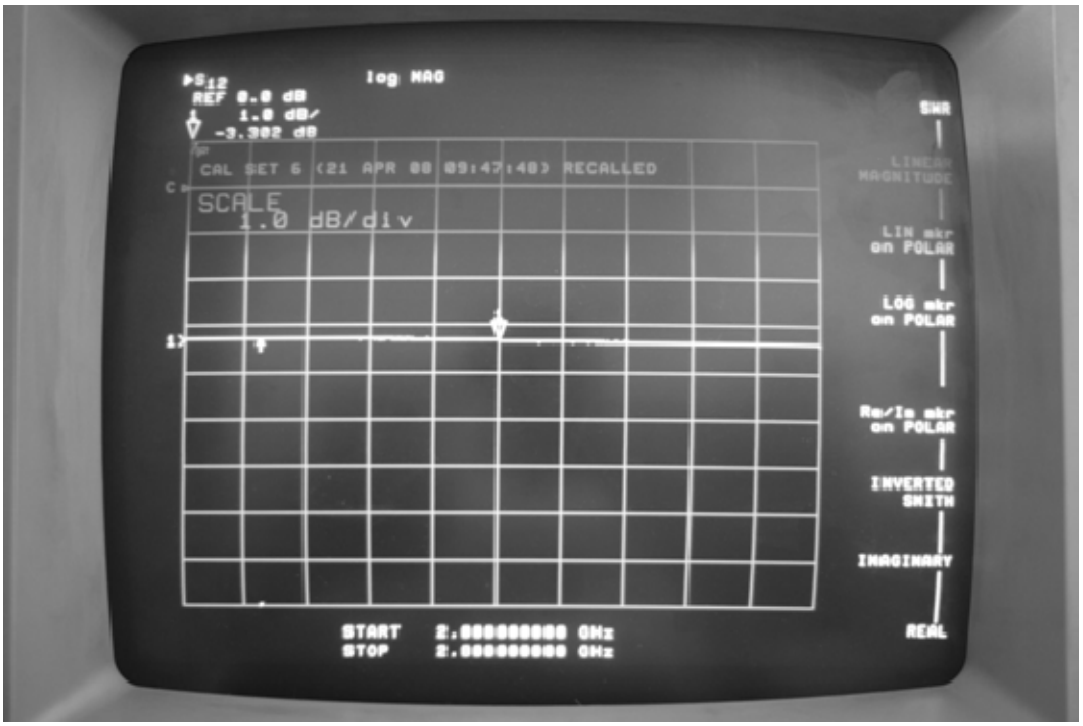

Figure 117. Splitter4; Port1; S12

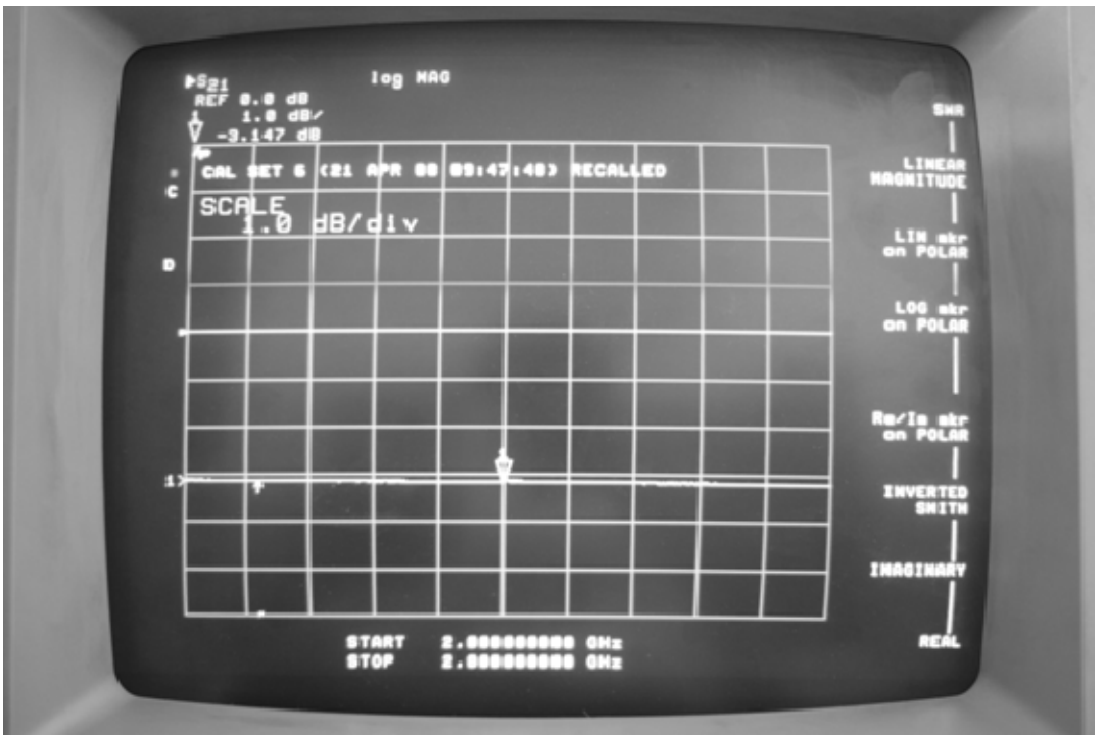

Figure 118. Splitter4; Port1; S21

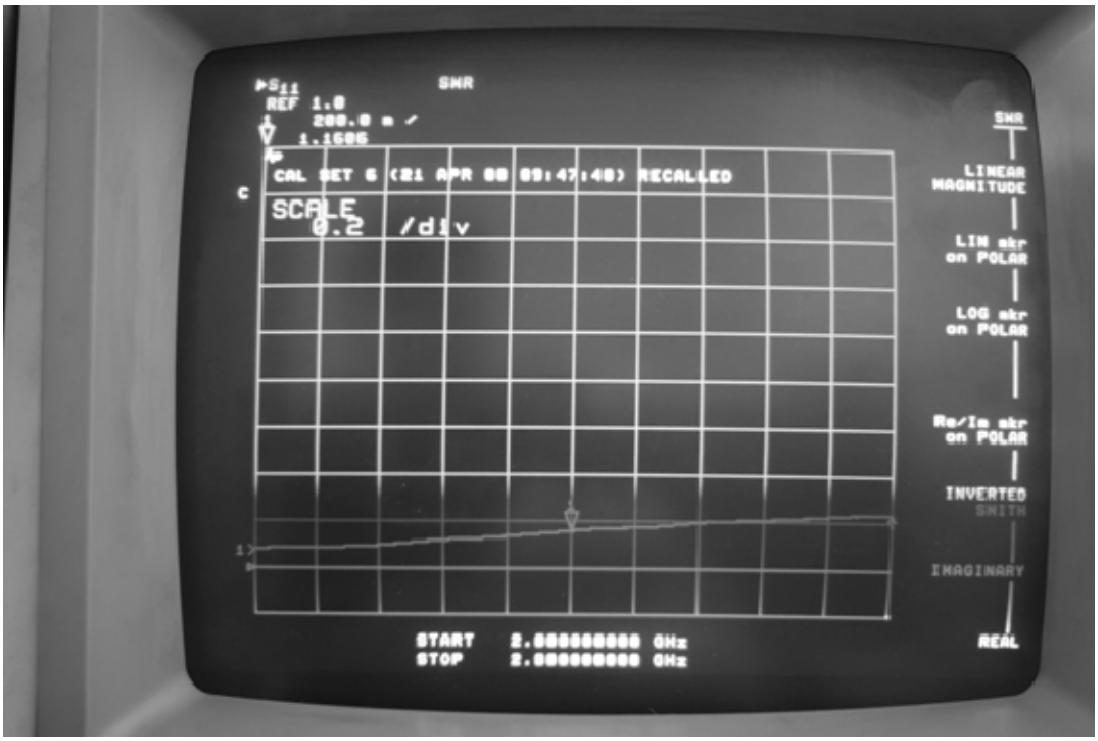

Figure 119. Splitter4; Port2; S11

Figure 120. Splitter4; Port2; S22

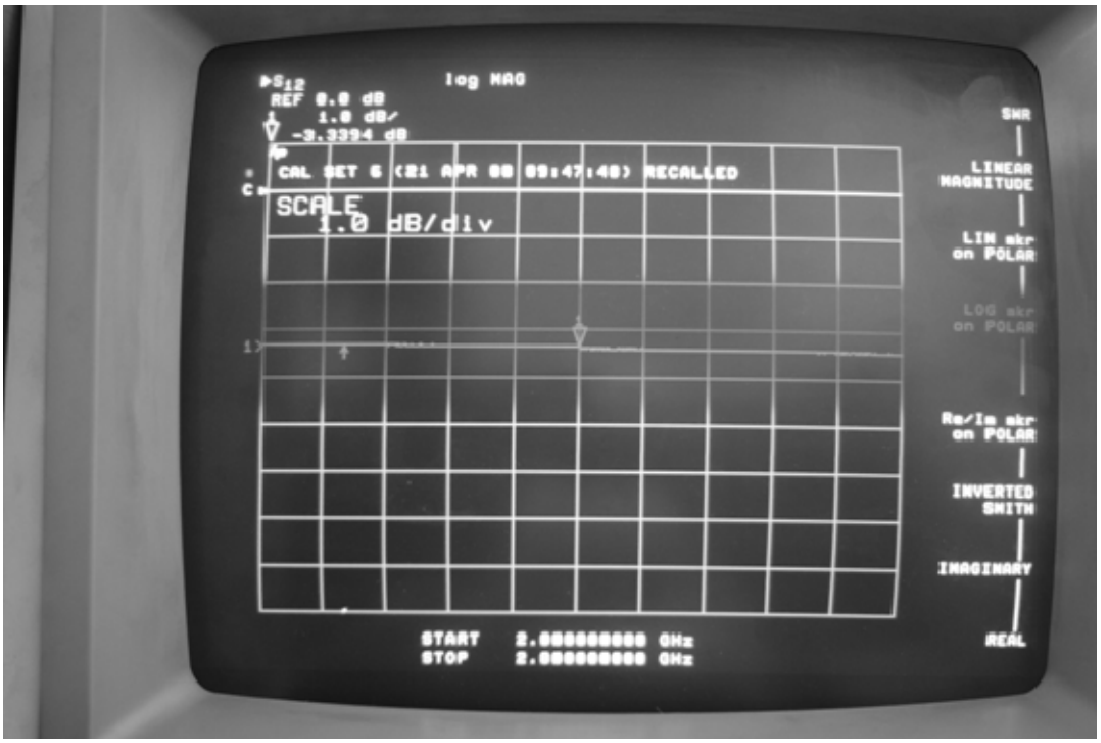

Figure 121. Splitter4; Port2; S12

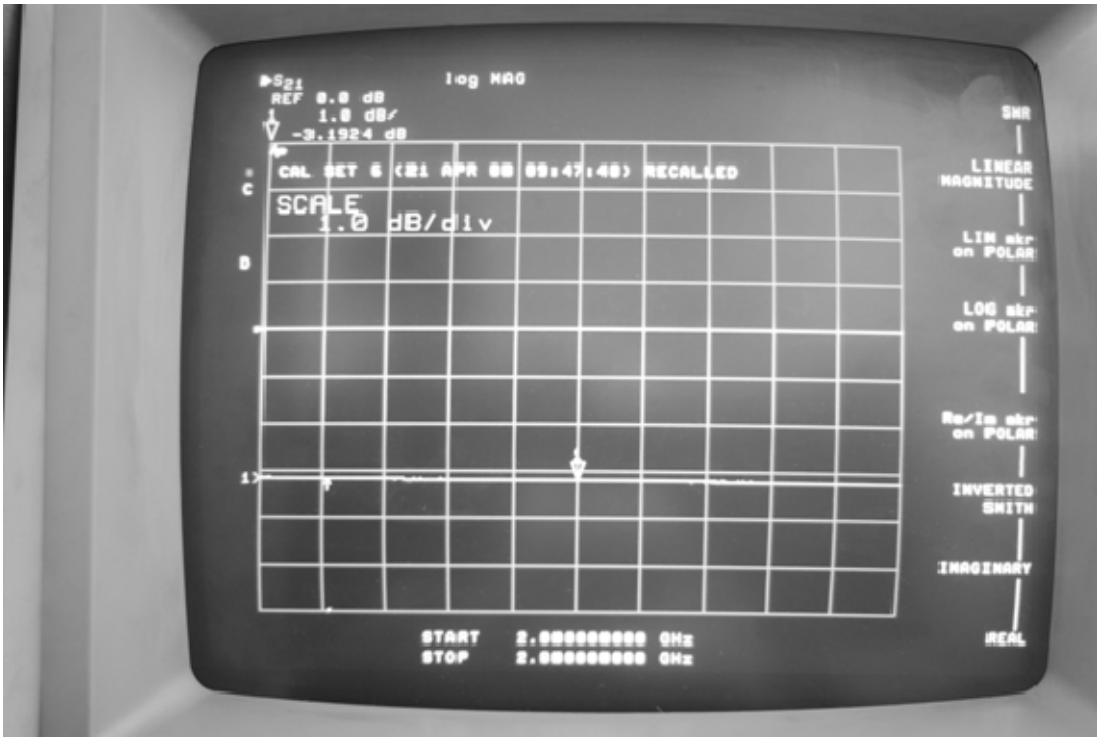

Figure 122. Splitter4; Port2; S21

E. SWITCH 3

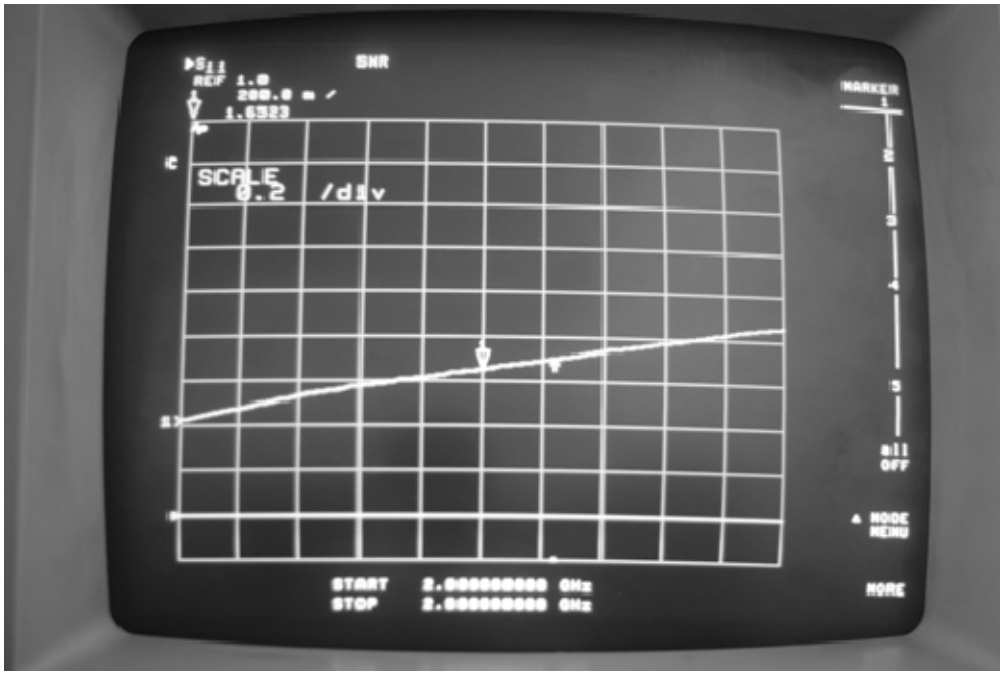

Figure 123. Switch3; Port1; S11

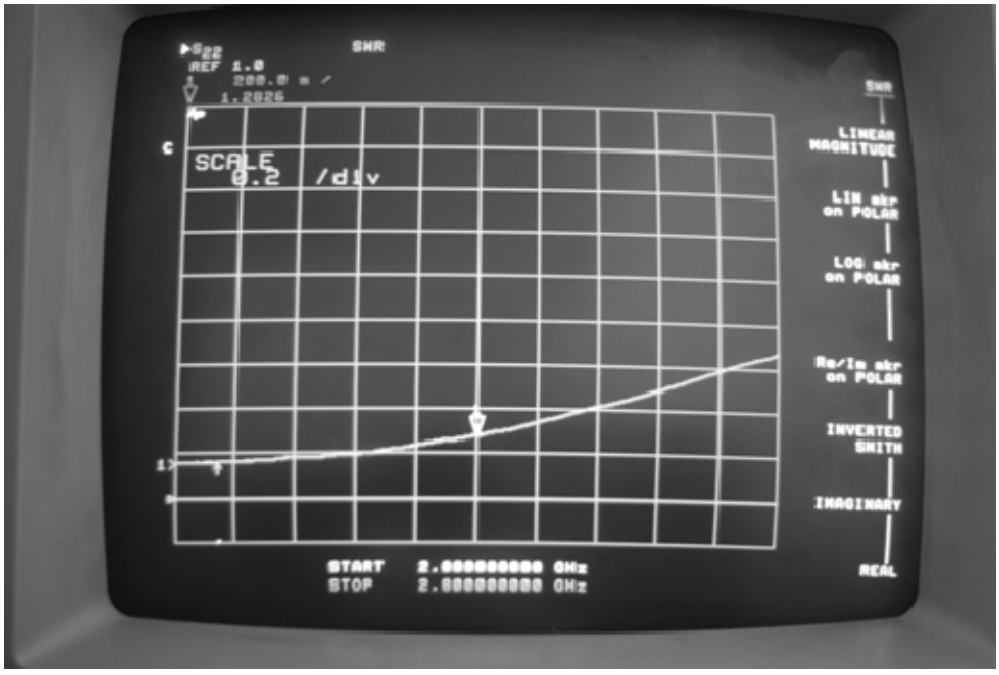

Figure 124. Switch3; Port1; S22

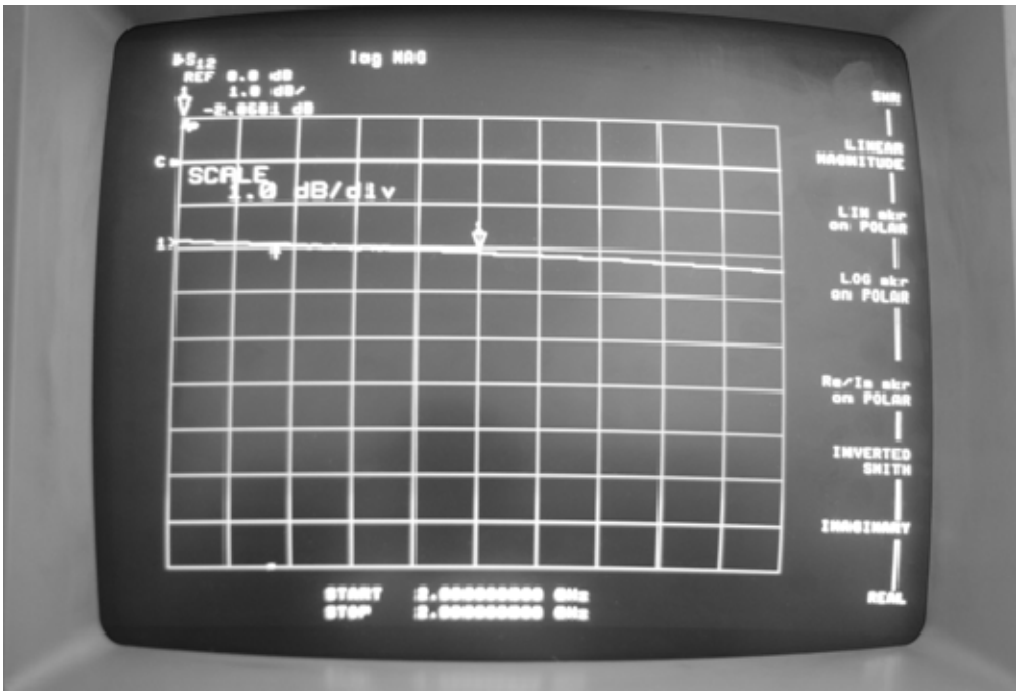

Figure 125. Switch3; Port1; S12

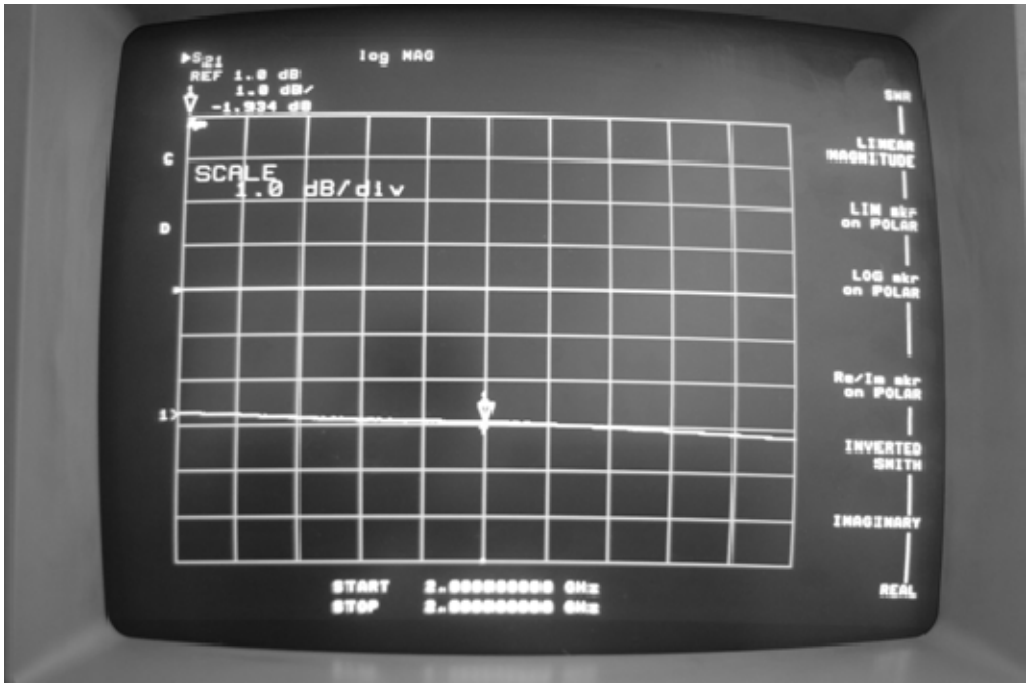

Figure 126. Switch3; Port1; S21

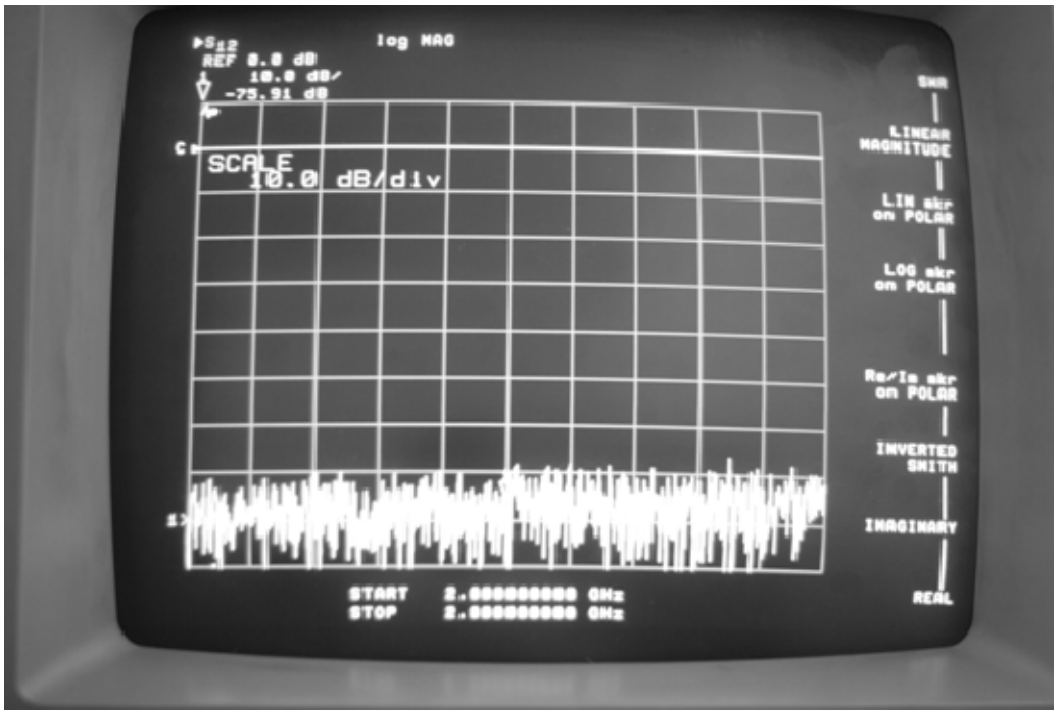

Figure 127. Switch3; Port1; S12; Port1-CLOSED

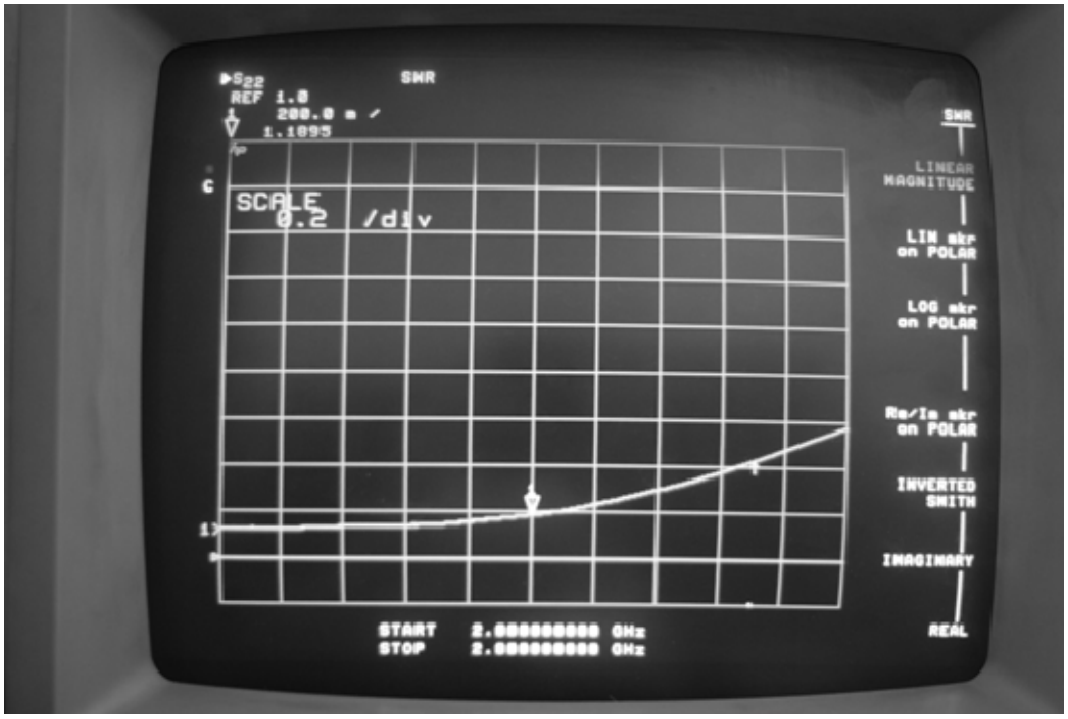

Figure 128. Switch3; Port2; S22

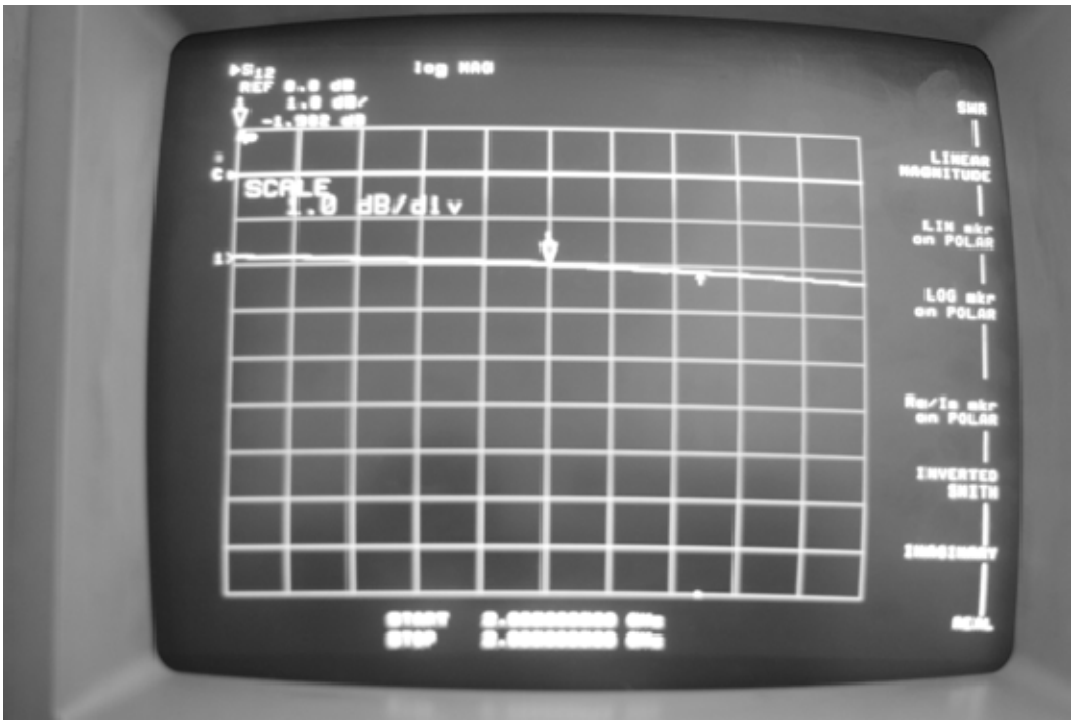

Figure 129. Switch3; Port2; S12

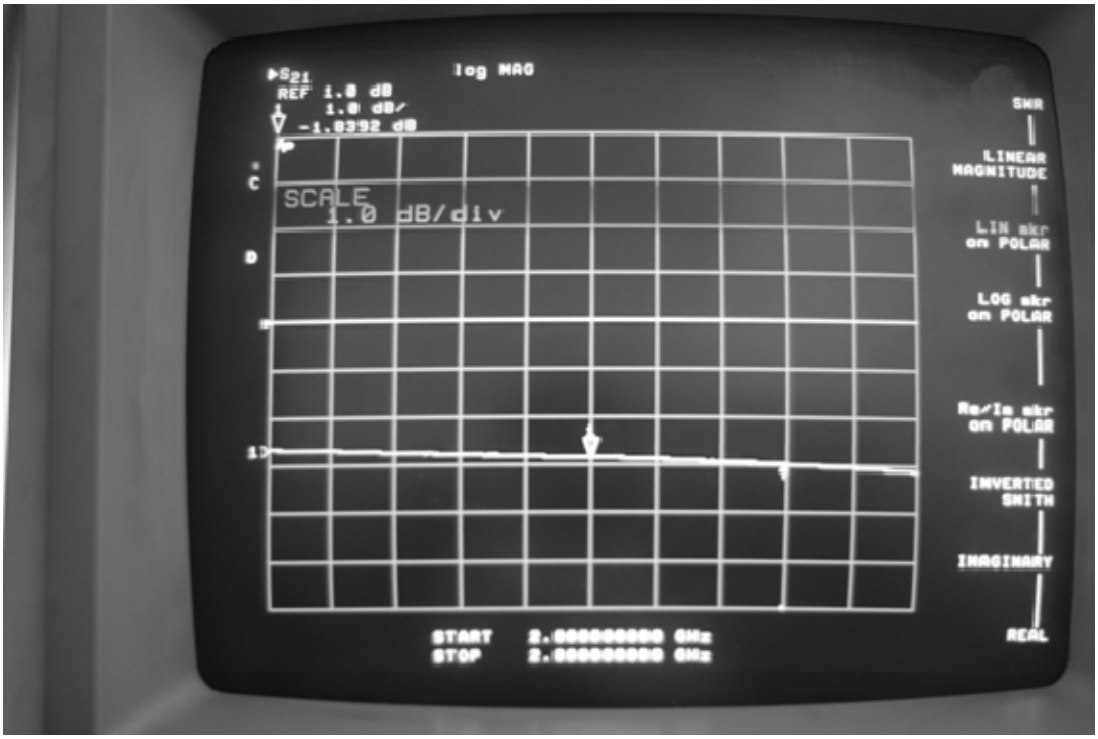

Figure 130. Switch3; Port2; S21

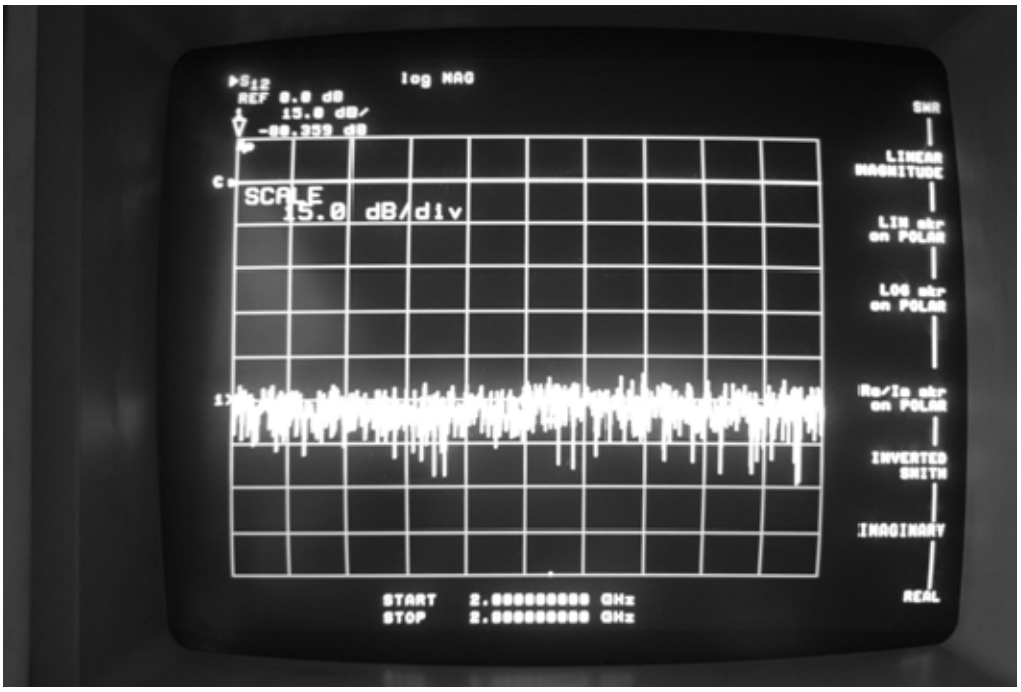

Figure 131. Switch3; Port2; S12; Port2-CLOSED

F. SWITCH 5

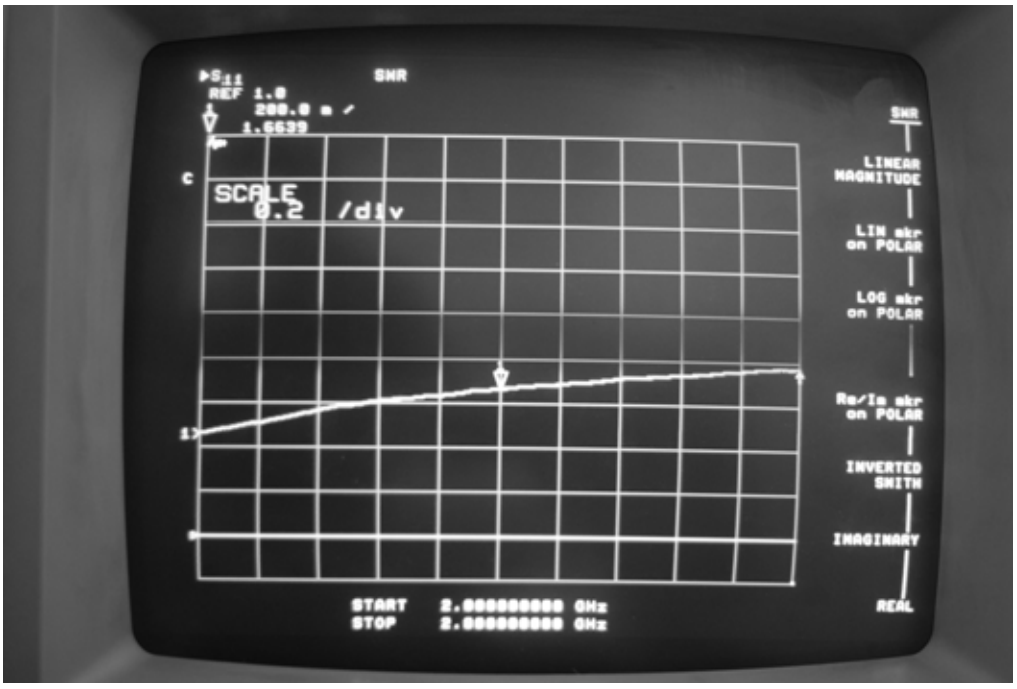

Figure 132. Switch5; Port1; S11

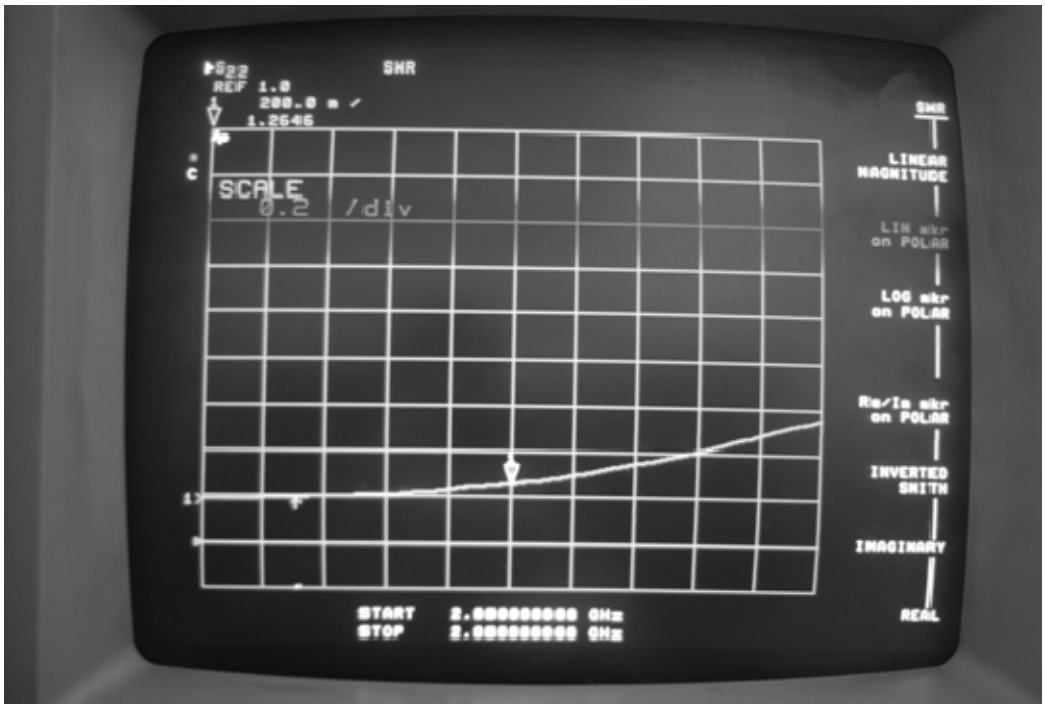

Figure 133. Switch5; Port1; S22

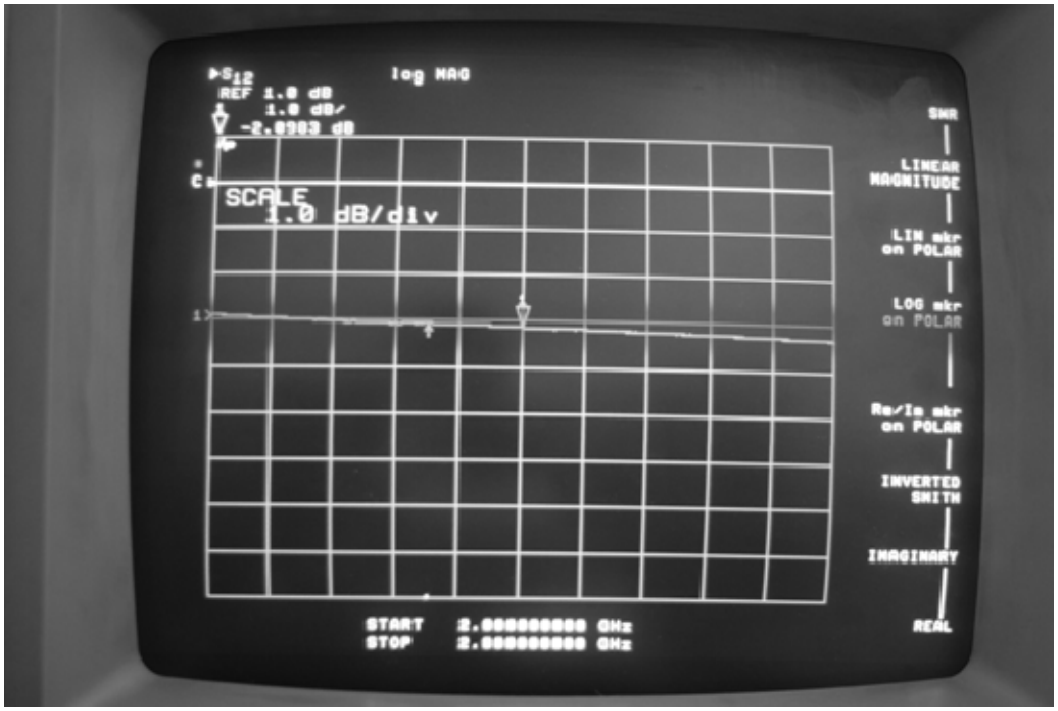

Figure 134. Switch5; Port1; S12

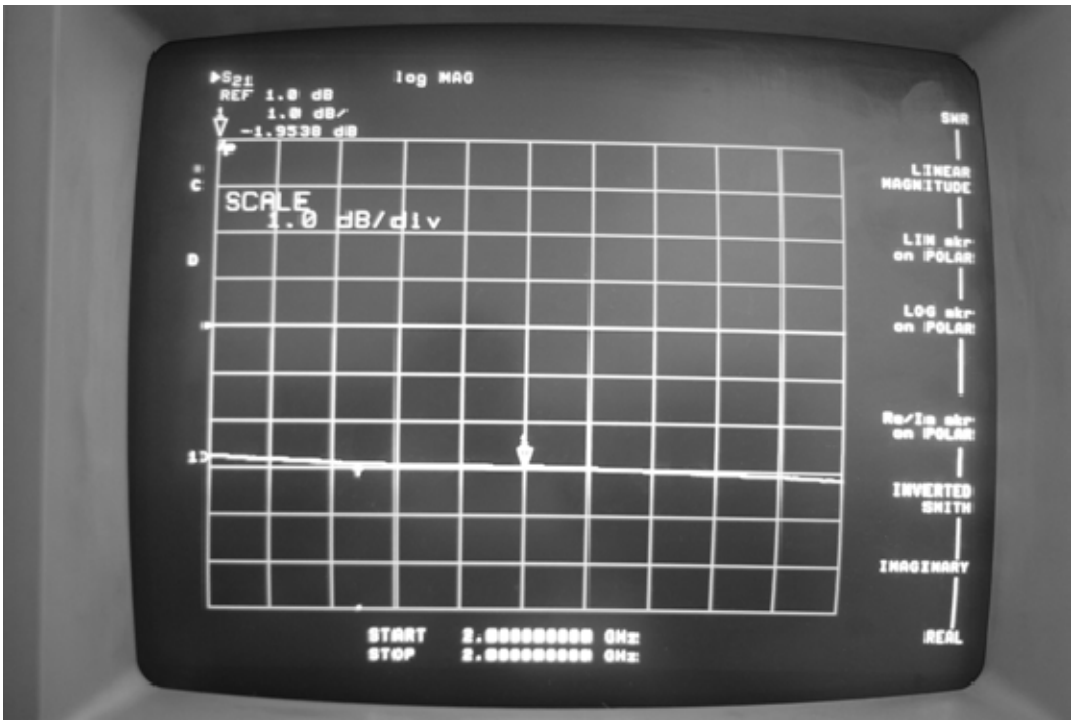

Figure 135. Switch5; Port1; S21

Figure 136. Switch5; Port1; S12; Port1-CLOSED

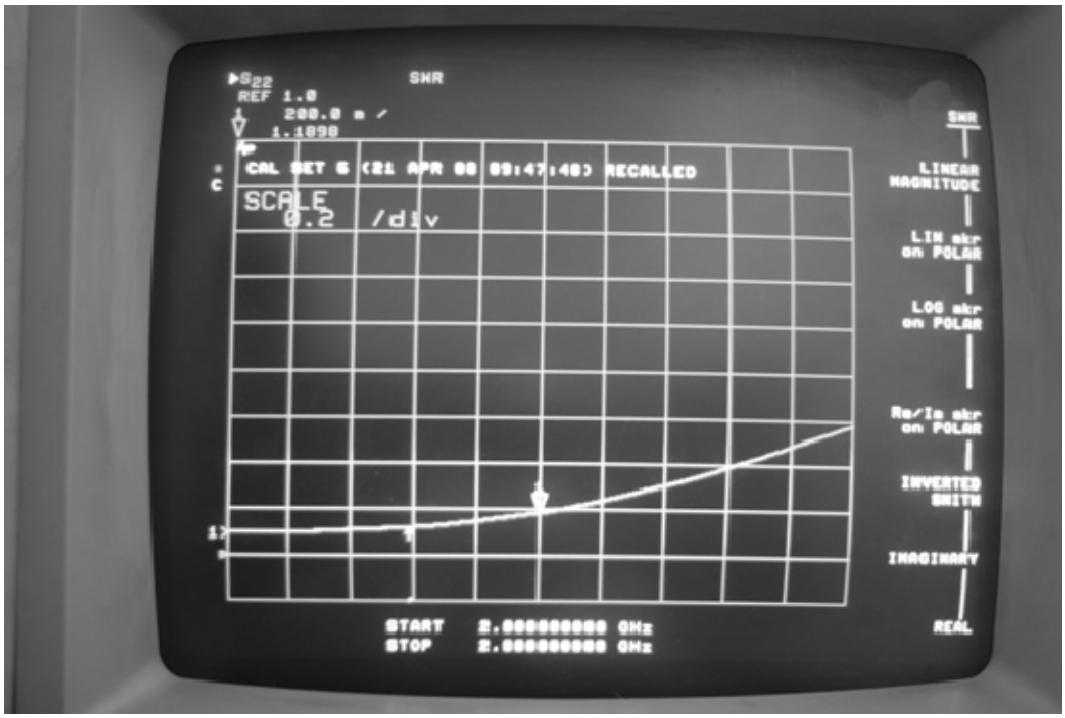

Figure 137. Switch5; Port2; S22

Figure 138. Switch5; Port2; S12

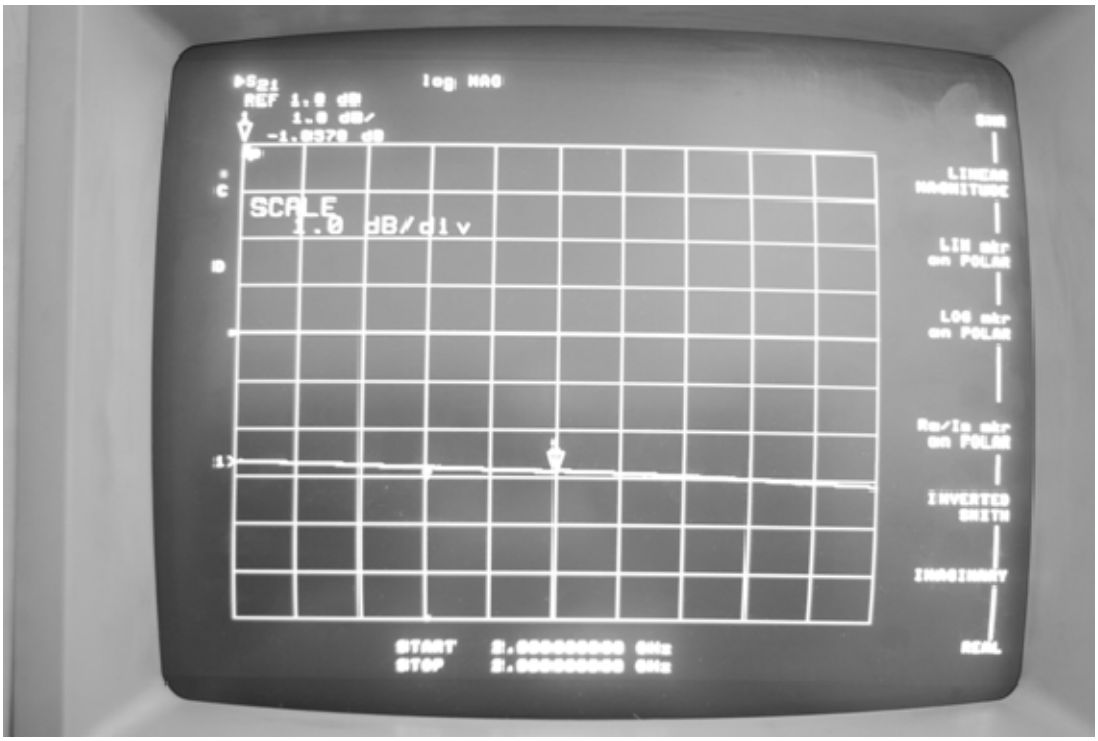

Figure 139. Switch5; Port2; S21

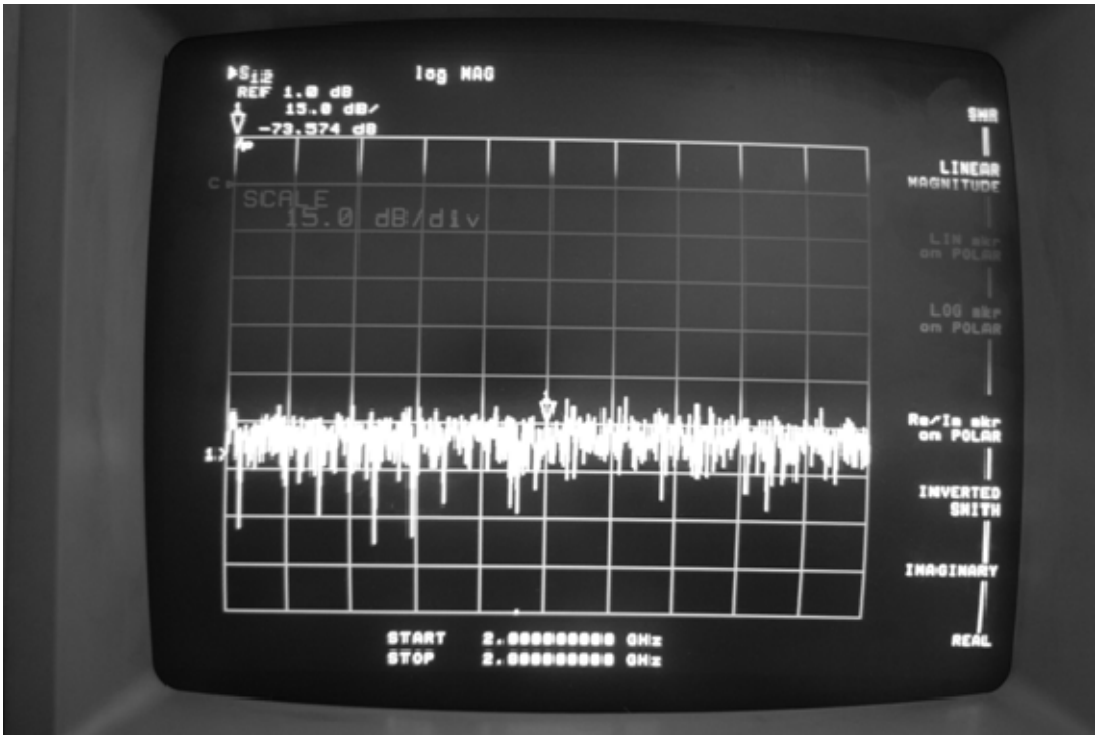

Figure 140. Switch5; Port2; S12; Port2-CLOSED

G. SWITCH 6

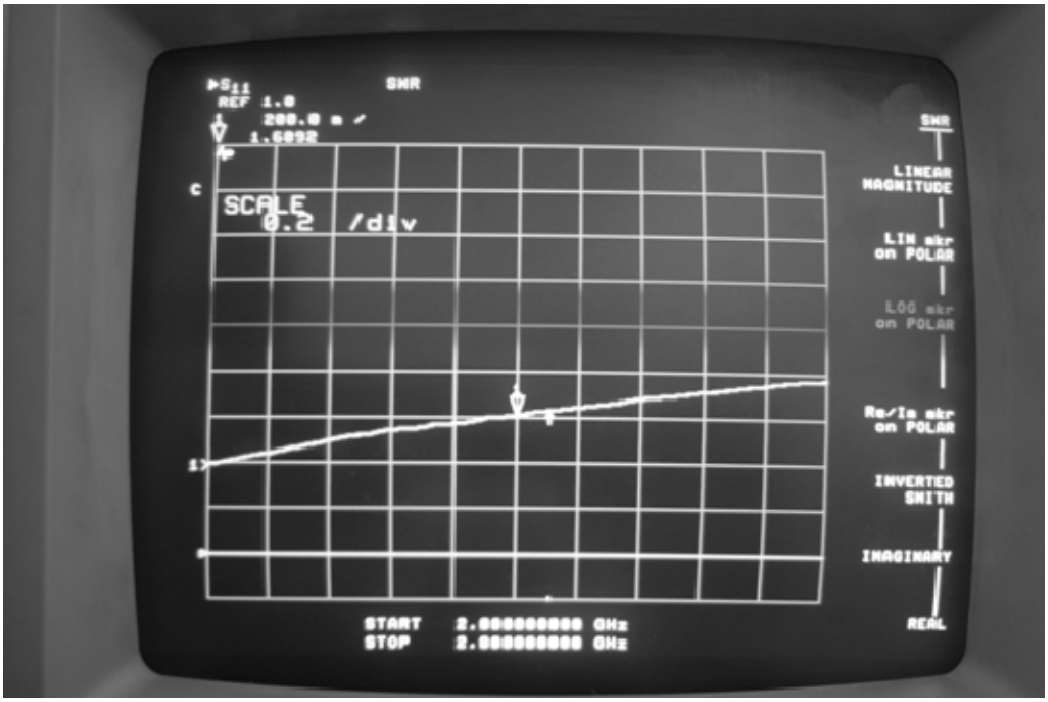

Figure 141. Switch6; Port1; S11

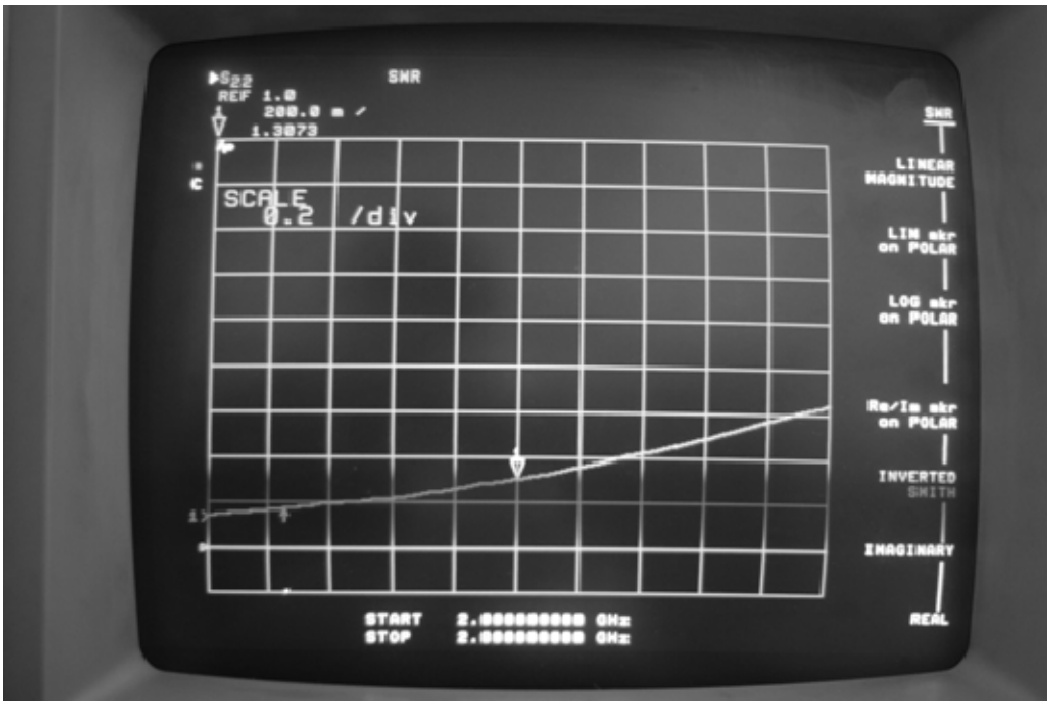

Figure 142. Switch6; Port1; S22

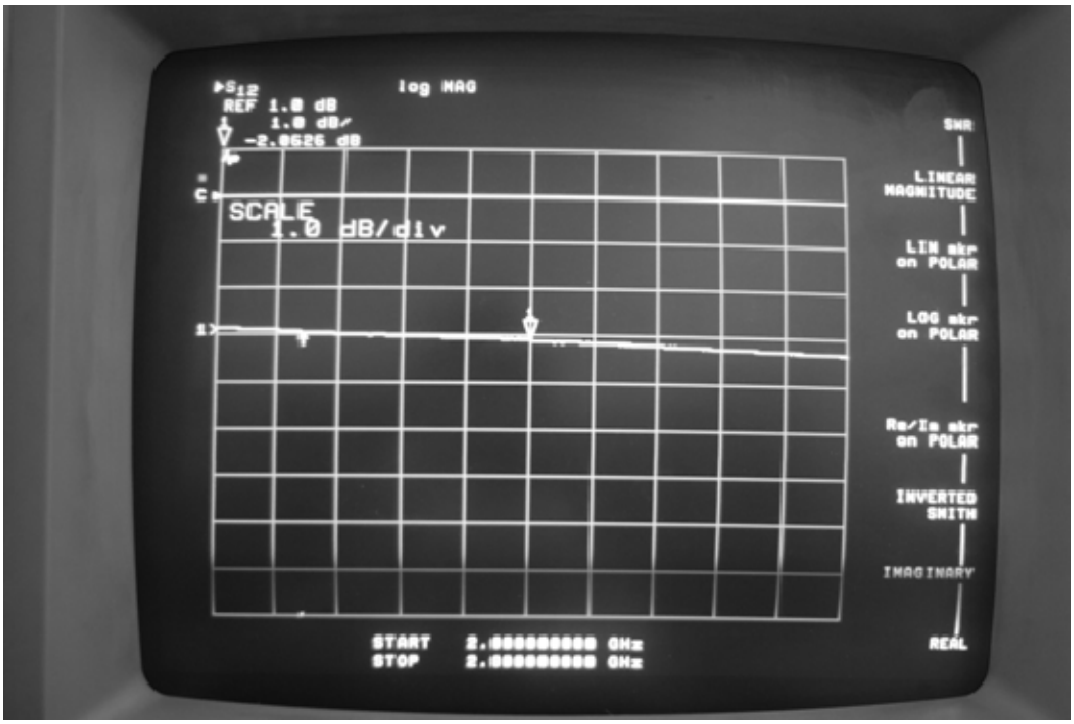

Figure 143. Switch6; Port1; S12

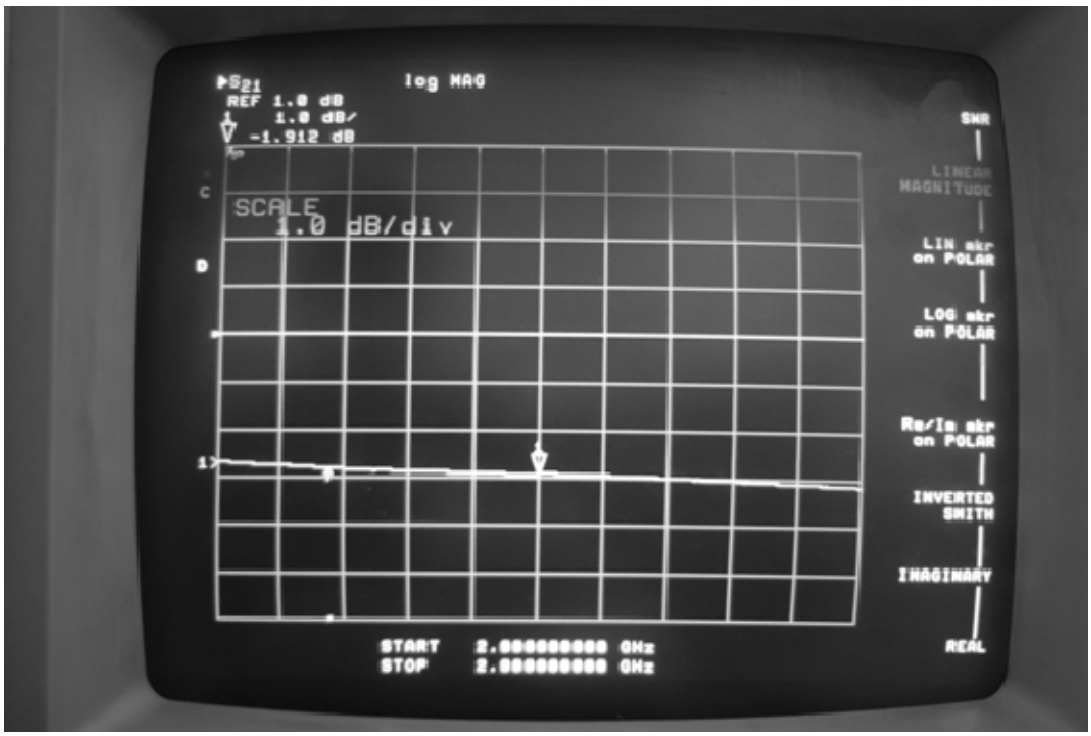

Figure 144. Switch6; Port1; S21

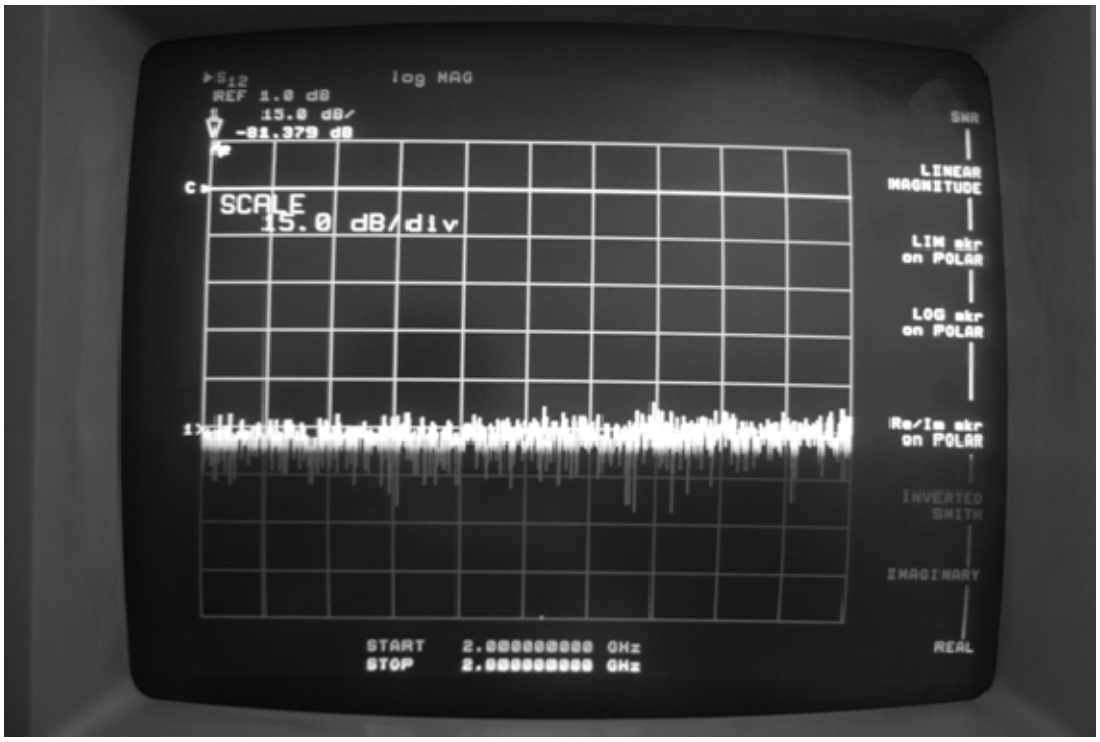

Figure 145. Switch6; Port1; S12; Port1-CLOSED

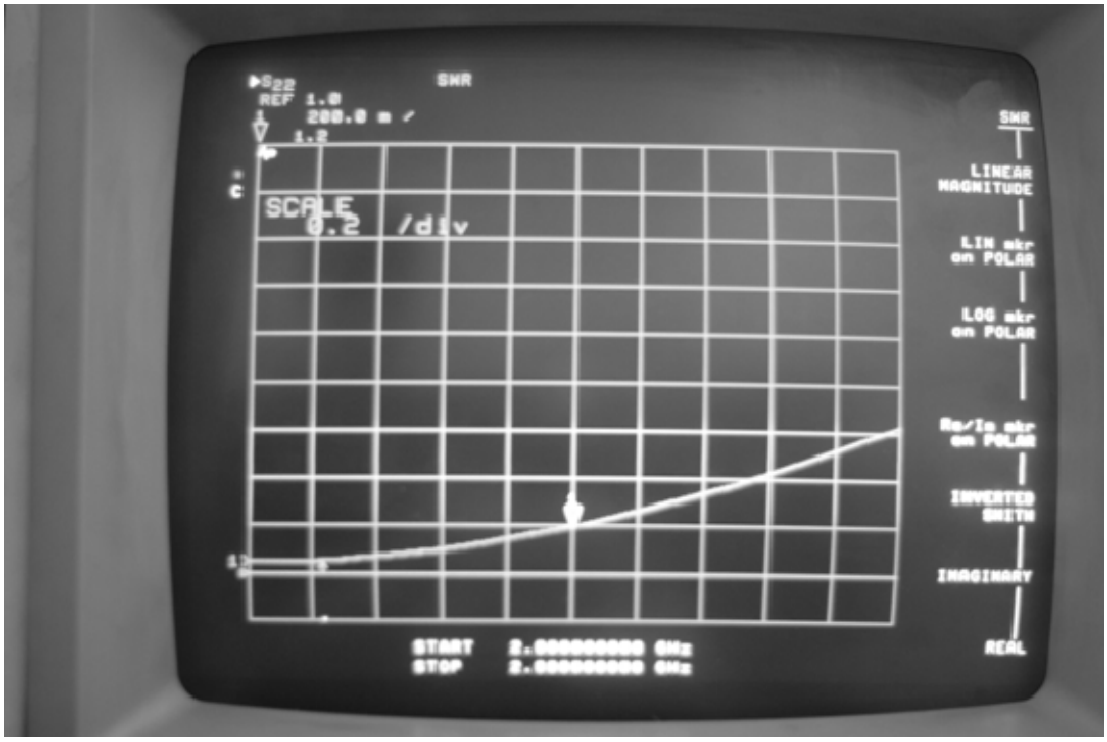

Figure 146. Switch6; Port2; S22

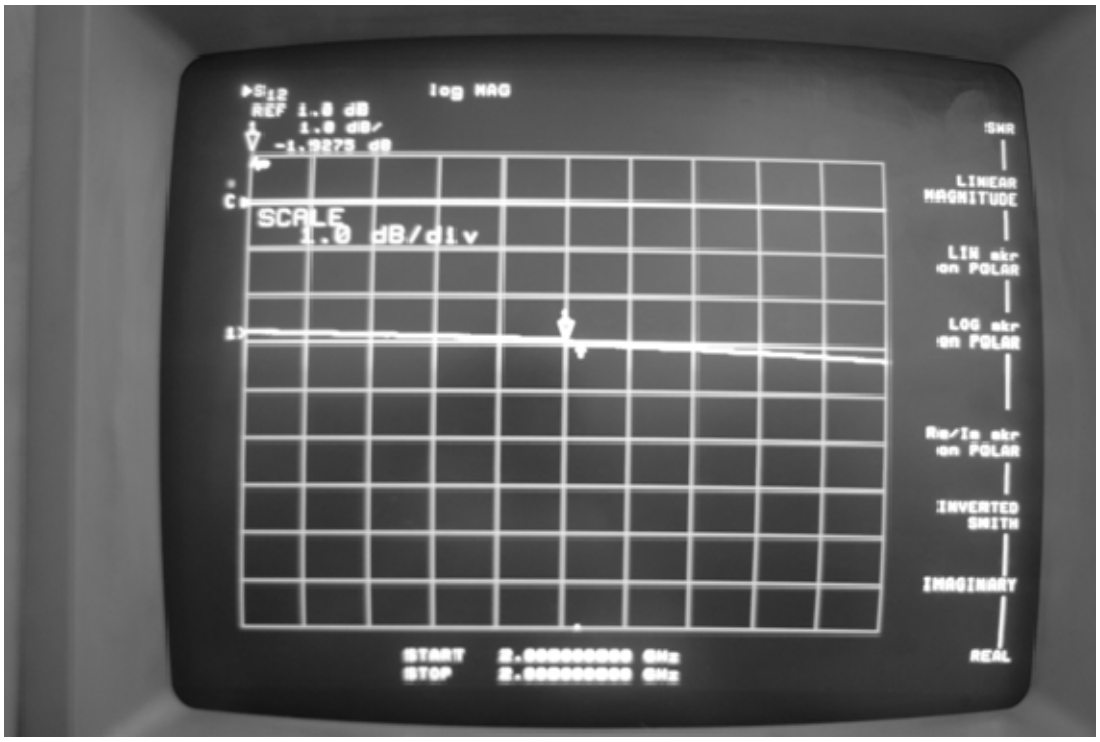

Figure 147. Switch6; Port2; S12

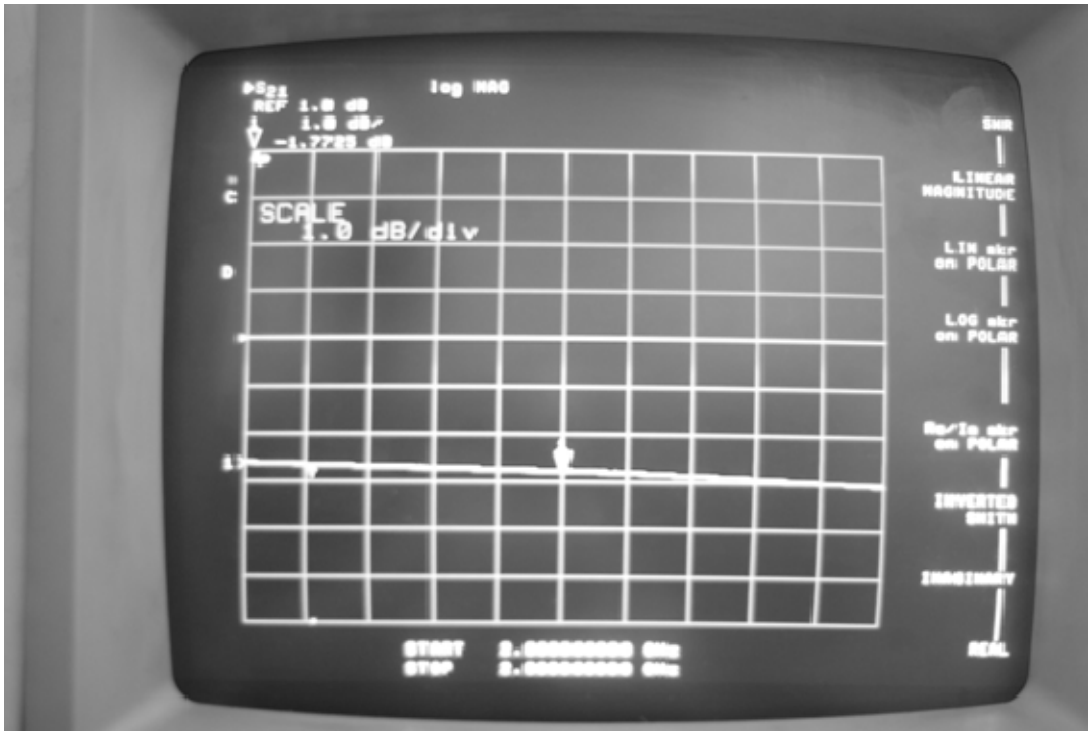

Figure 148. Switch6; Port2; S21

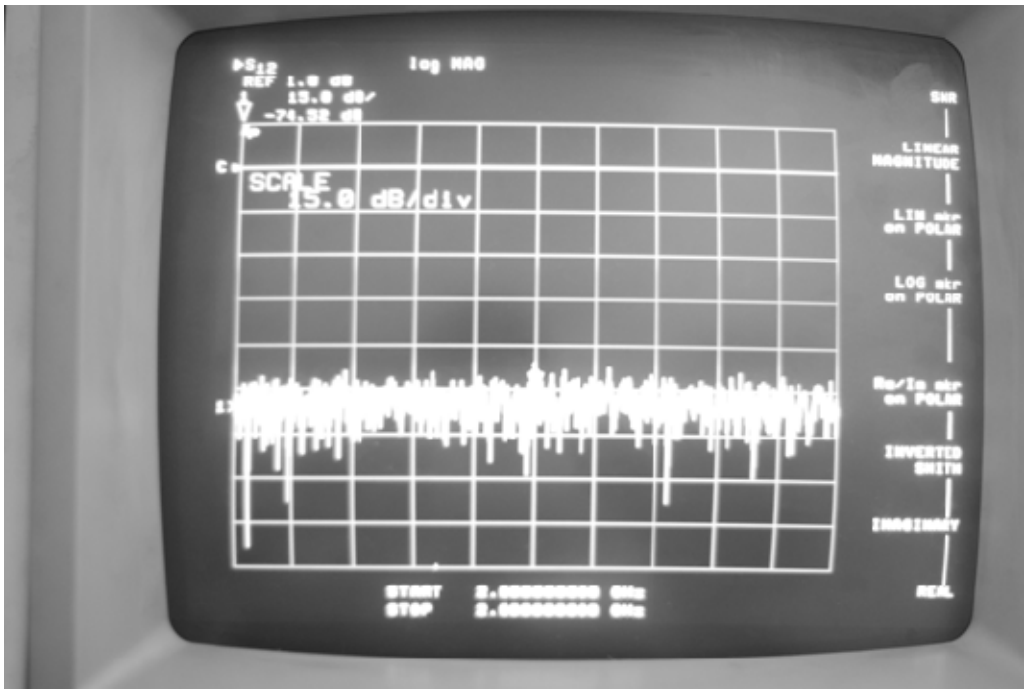

Figure 149. Switch6; Port2; S12; Port2-CLOSED

H. SWITCH 8

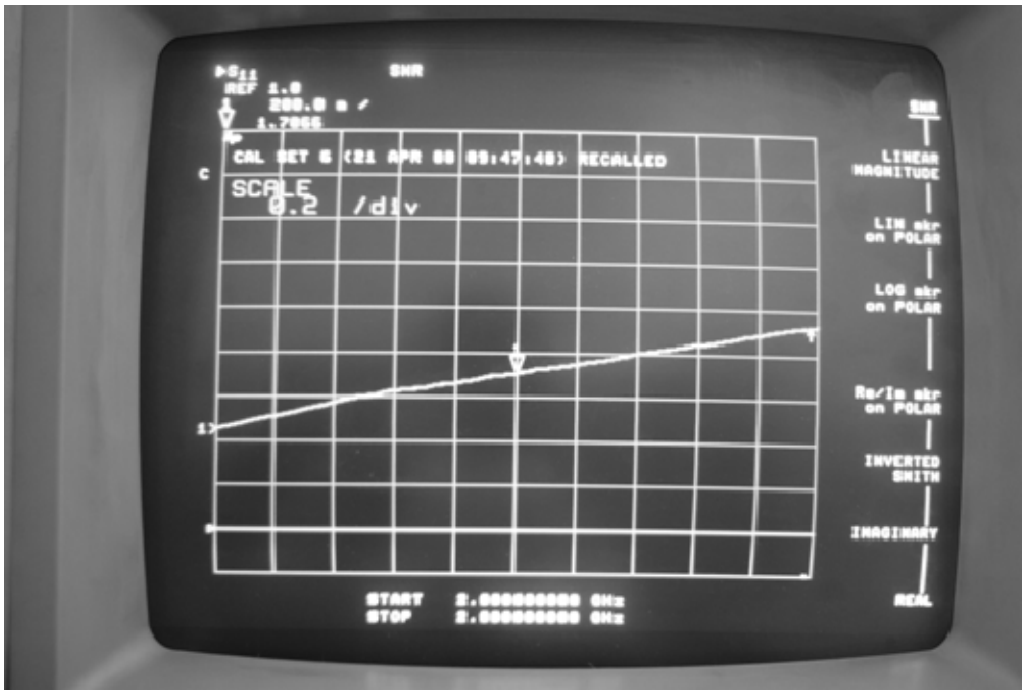

Figure 150. Switch8; Port1; S11

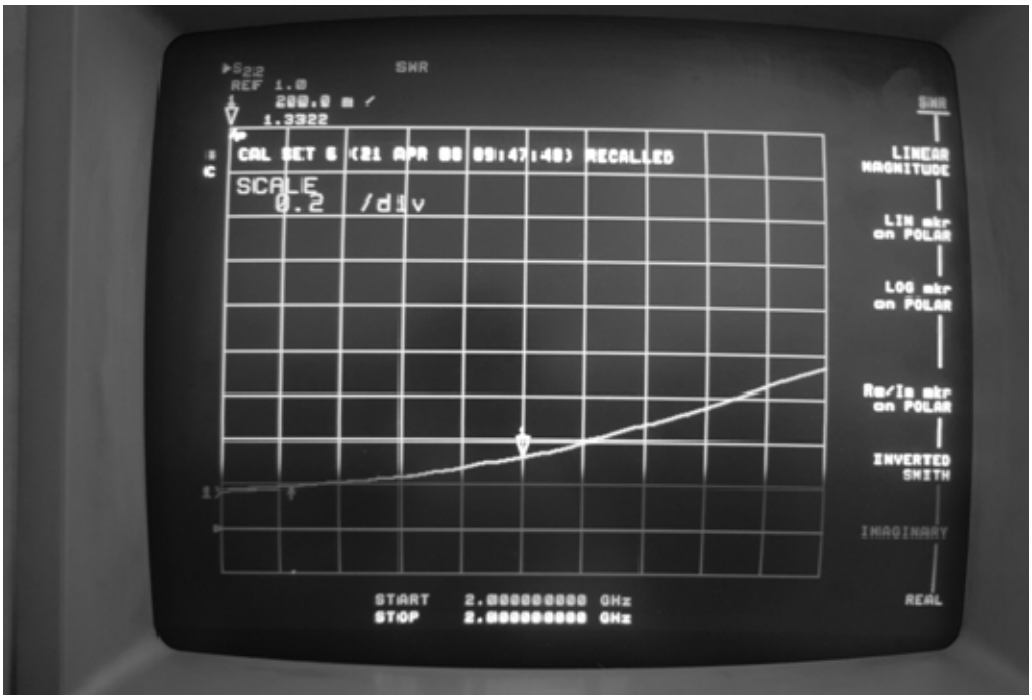

Figure 151. Switch8; Port1; S22

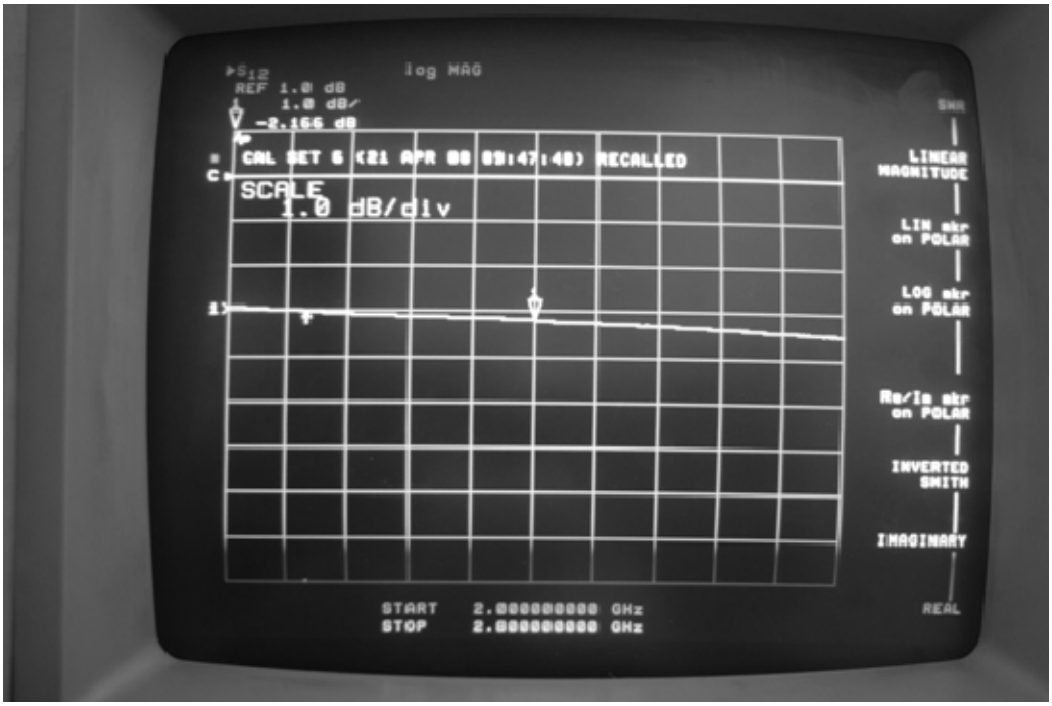

Figure 152. Switch8; Port1; S12

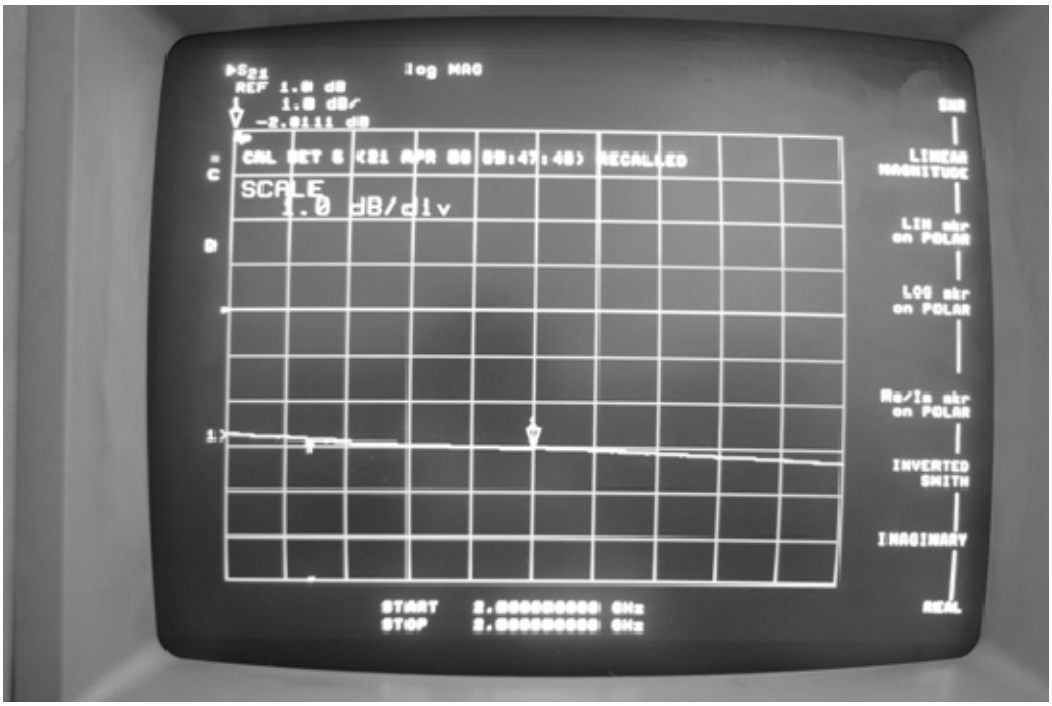

Figure 153. Switch8; Port1; S21

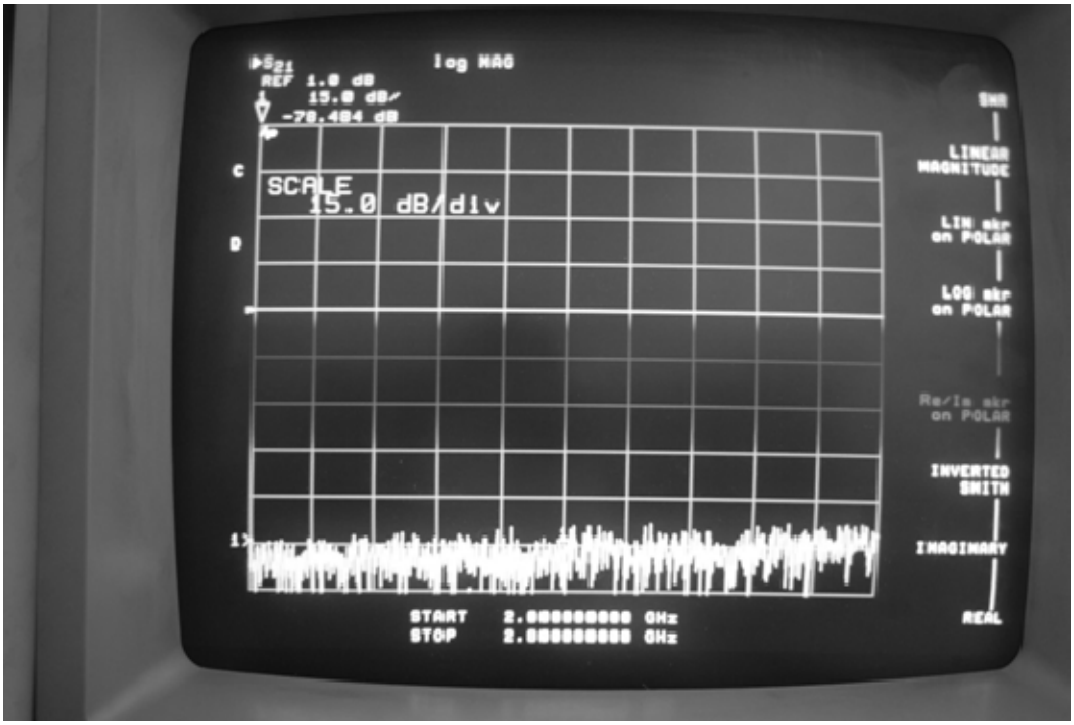

Figure 154. Switch8; Port1; S21; Port1-CLOSED

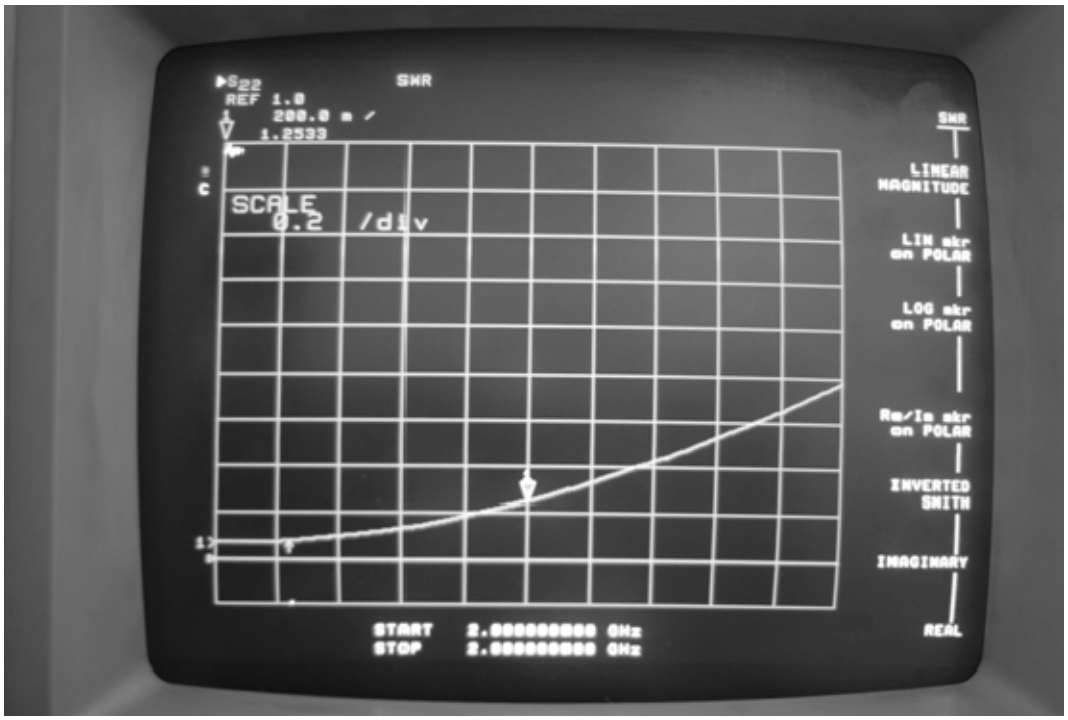

Figure 155. Switch8; Port2; S22

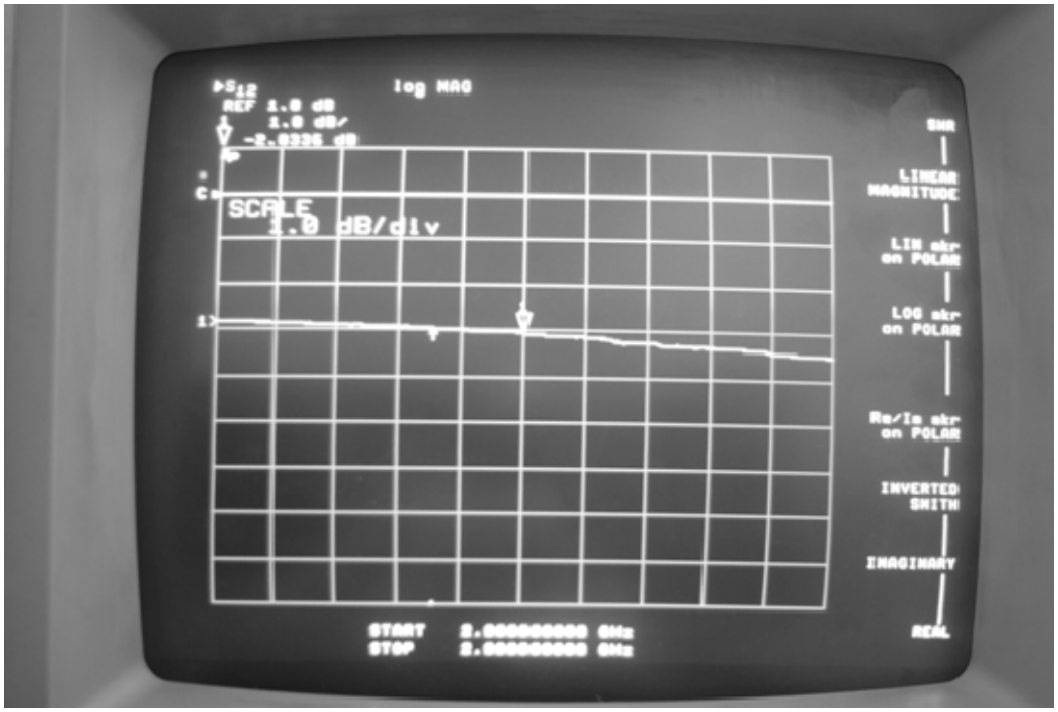

Figure 156. Switch8; Port2; S12

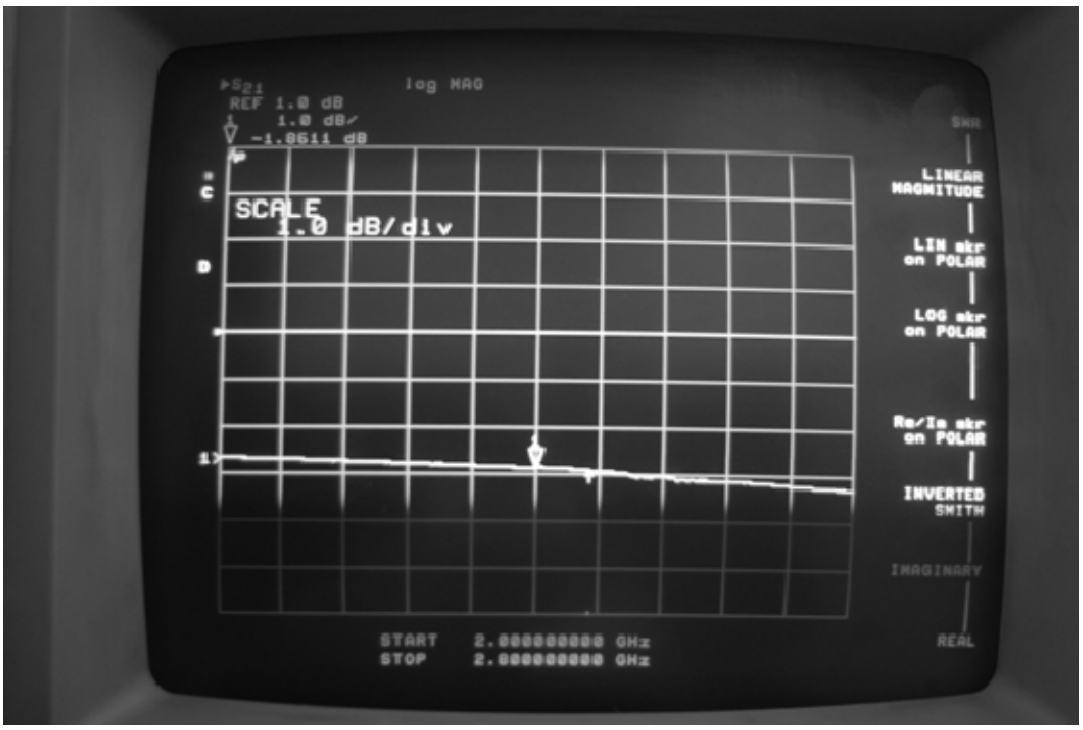

Figure 157. Switch8; Port2; S21

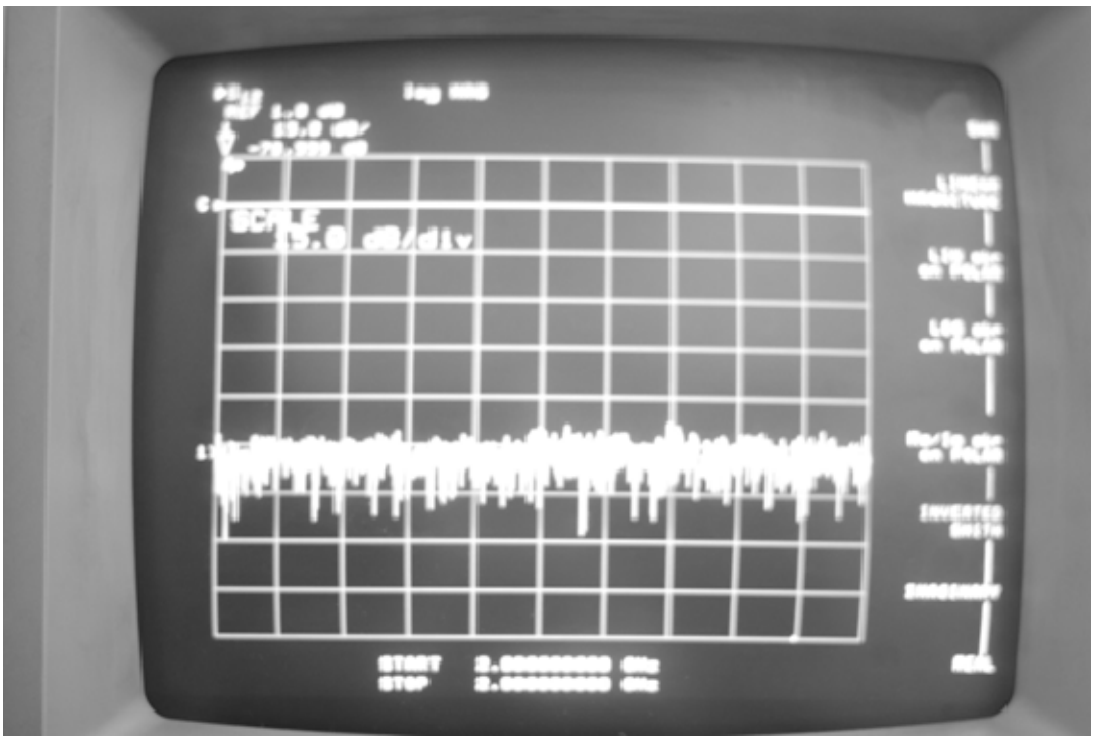

Figure 158. Switch8; Port2; S12; Port2-CLOSED

I. LNA 1

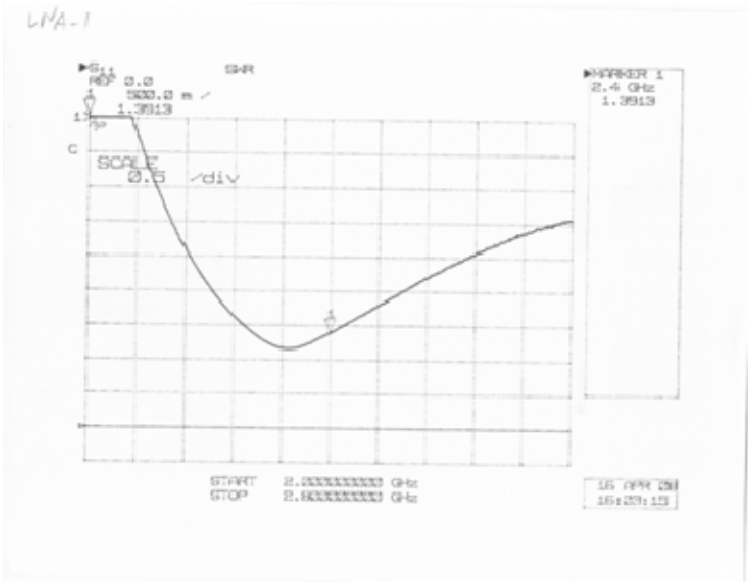

Figure 159. LNA1; S11

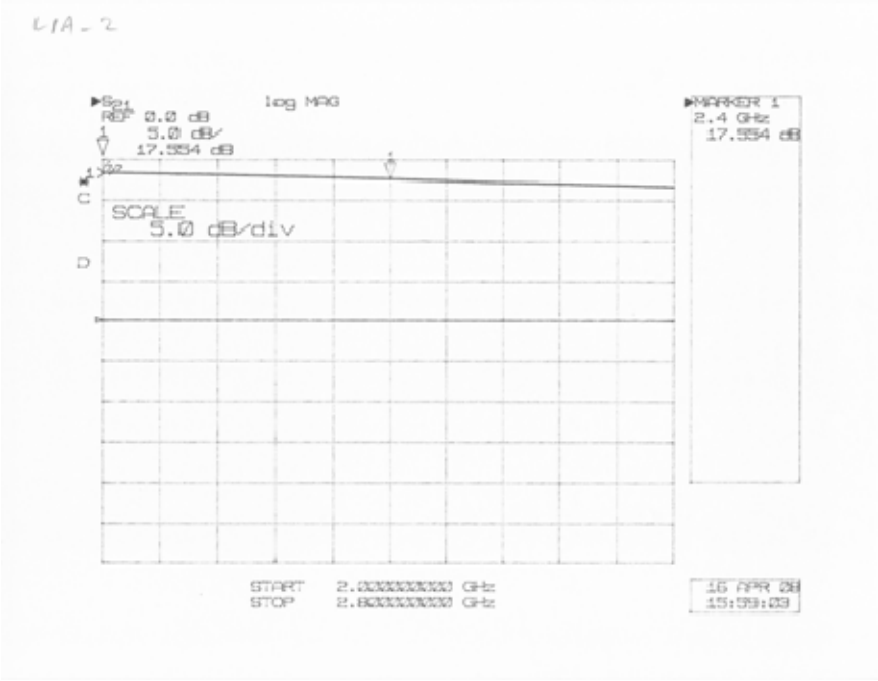

Figure 160. LNA1; S22

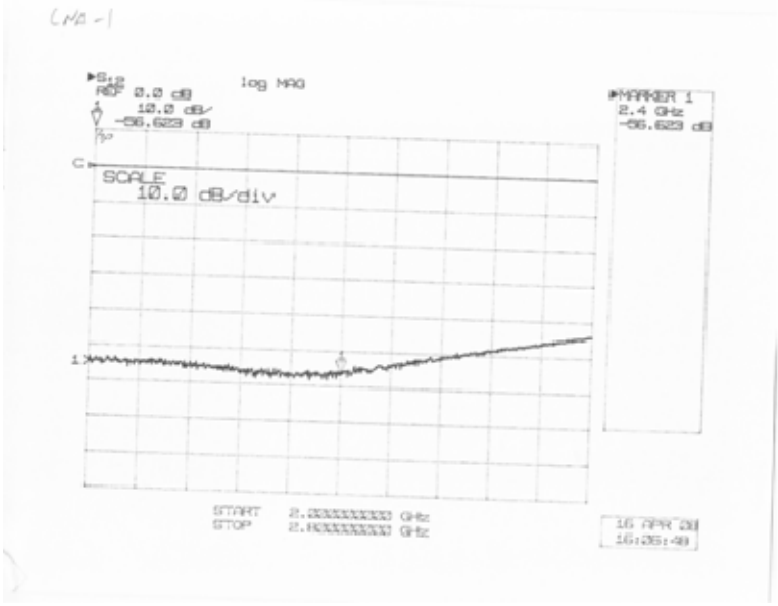

Figure 161. LNA1; S12

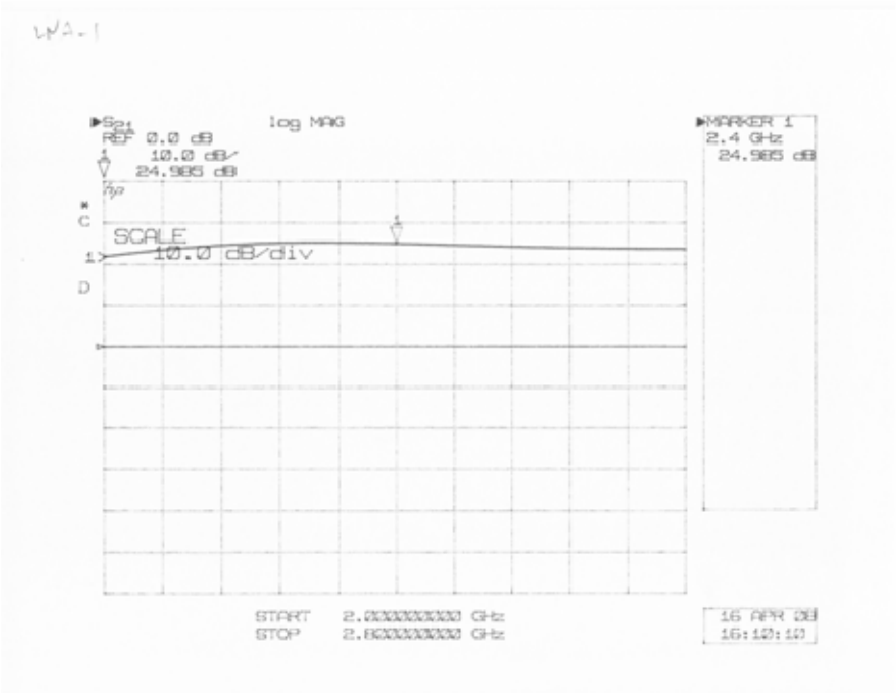

Figure 162. LNA1; S21

J. LNA 2

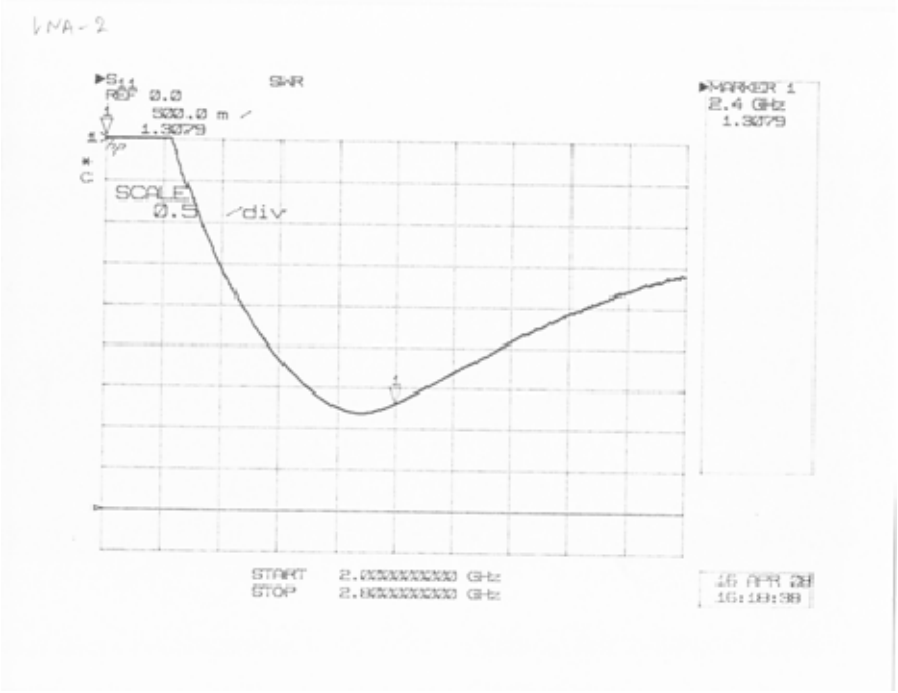

Figure 163. LNA2; S11

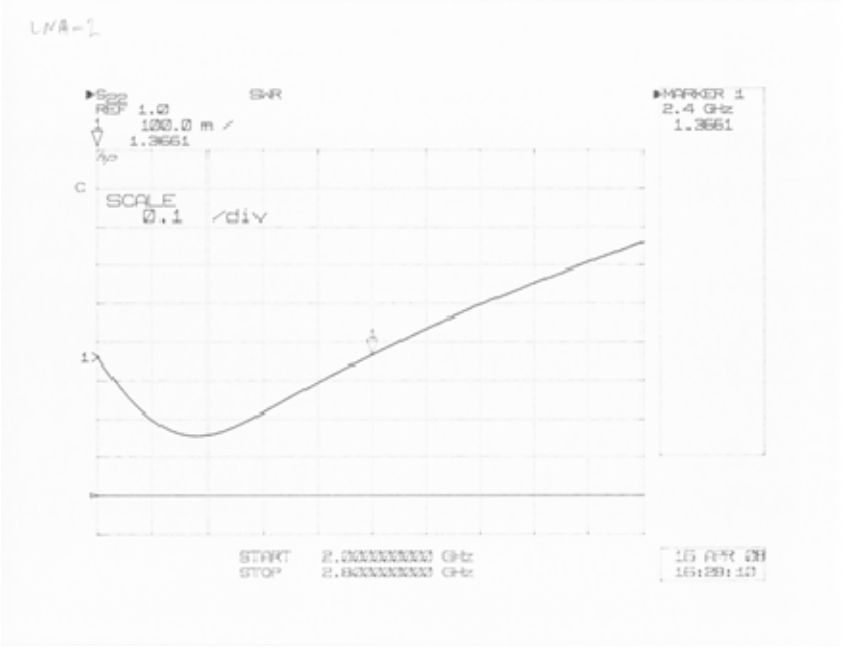

Figure 164. LNA2; S22

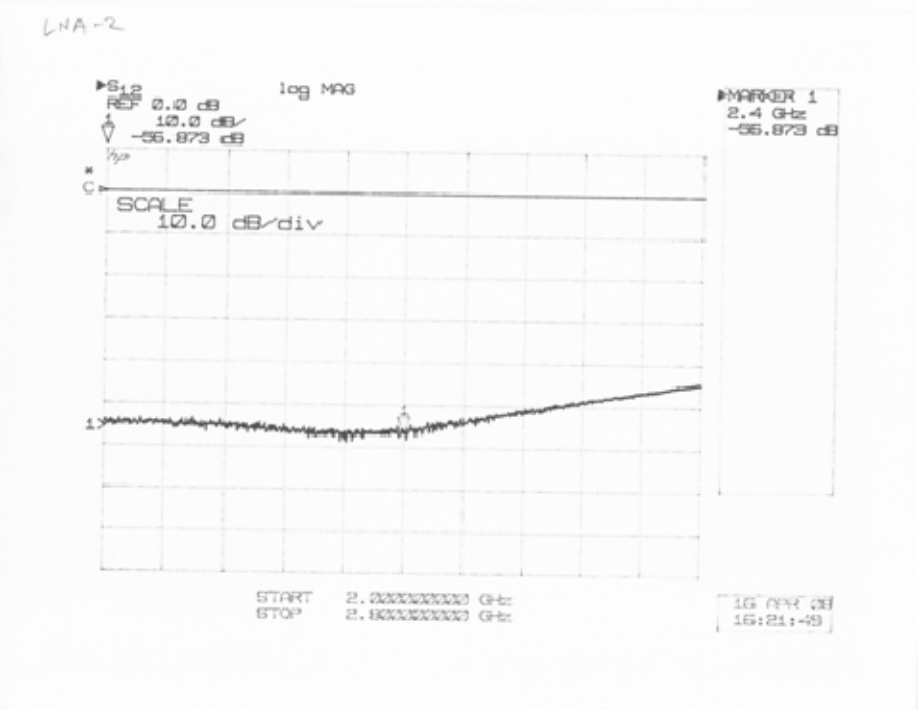

Figure 165. LNA2; S12

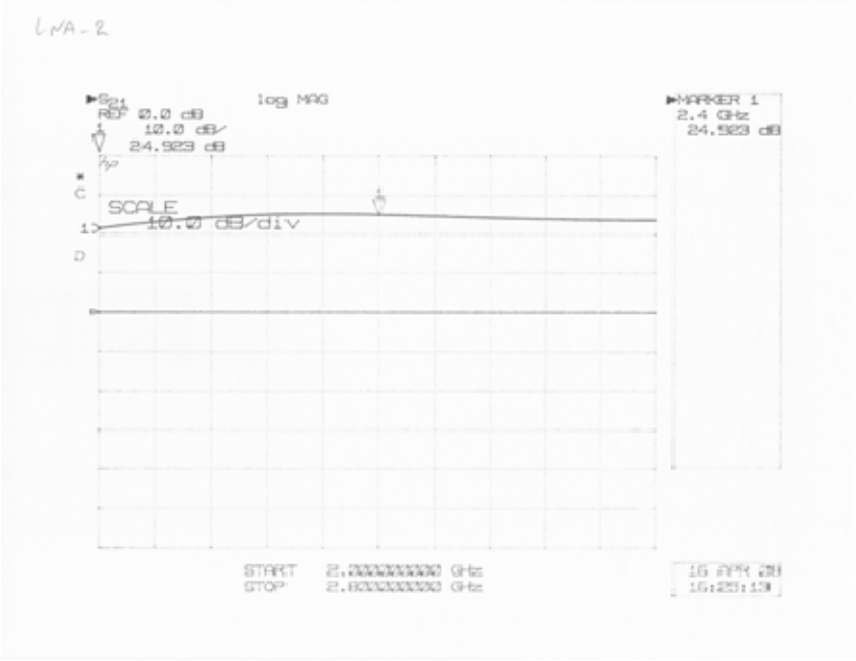

Figure 166. LNA2; S21

K. LPA 1

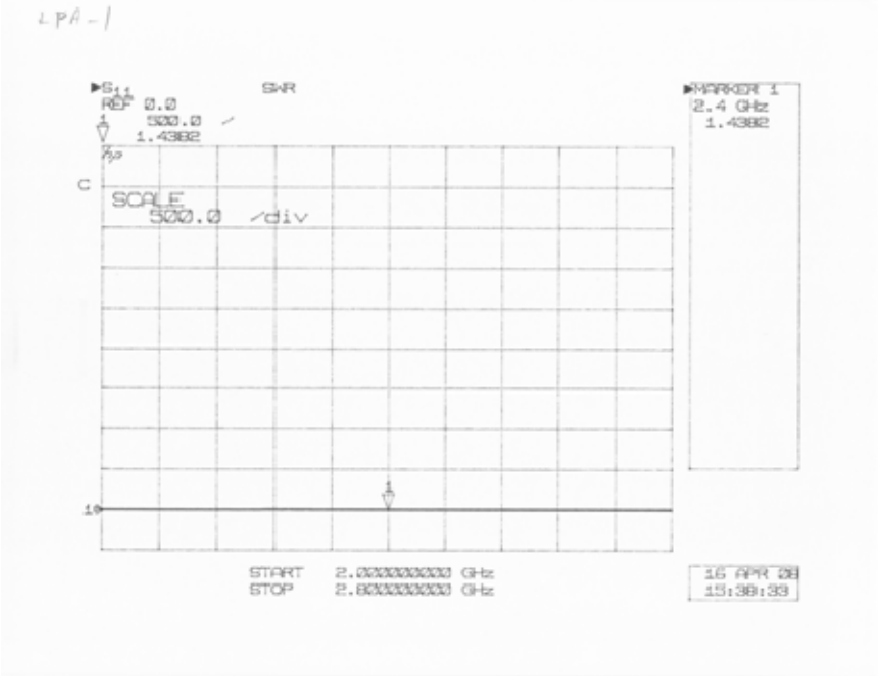

Figure 167. LPA1; S11

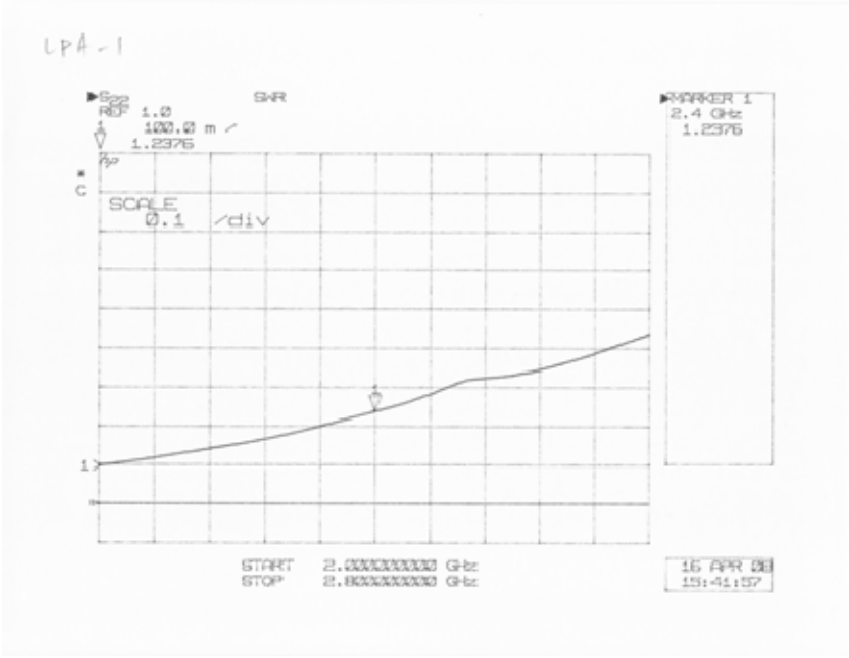

Figure 168. LPA1; S22

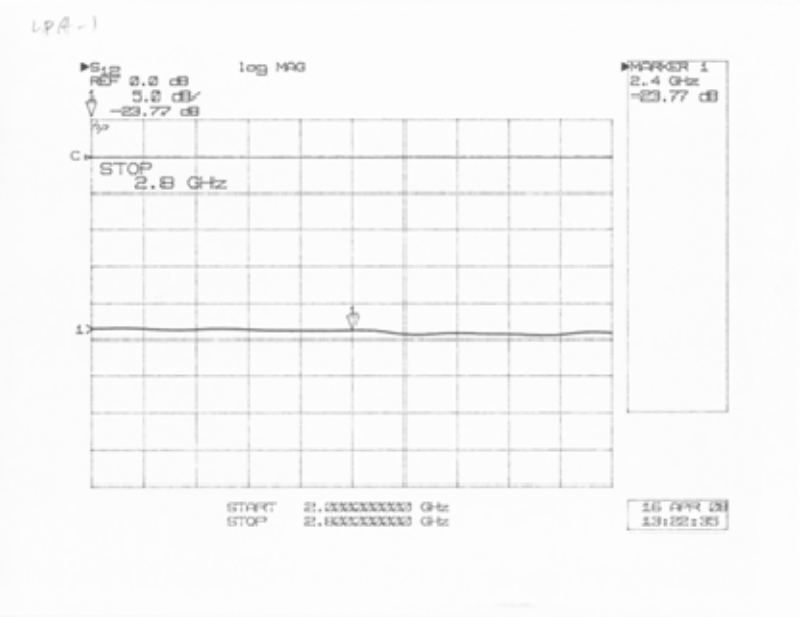

Figure 169. LPA1; S12

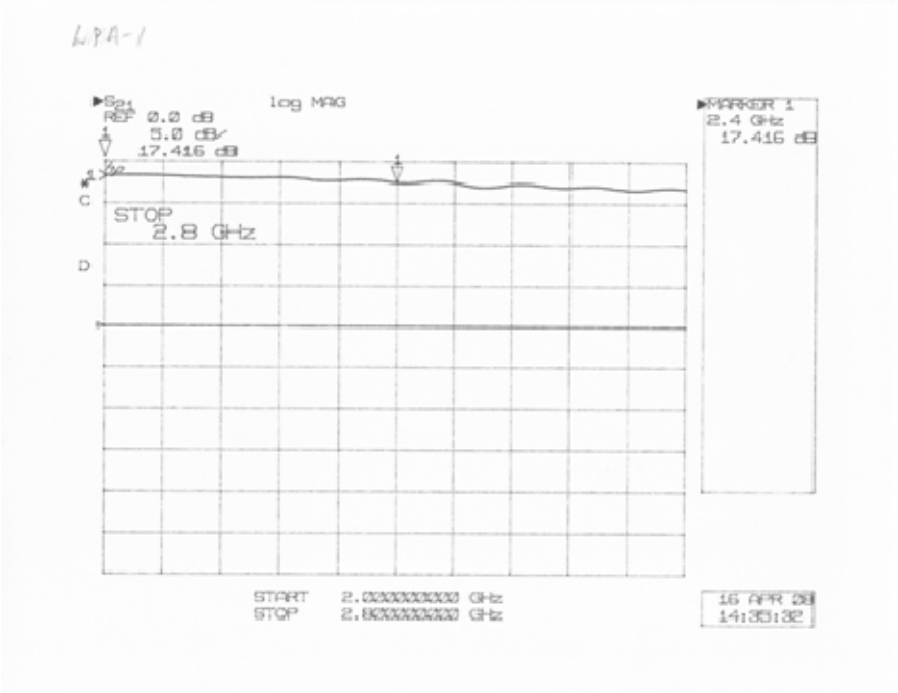

Figure 170. LPA1; S21

L. LPA 2

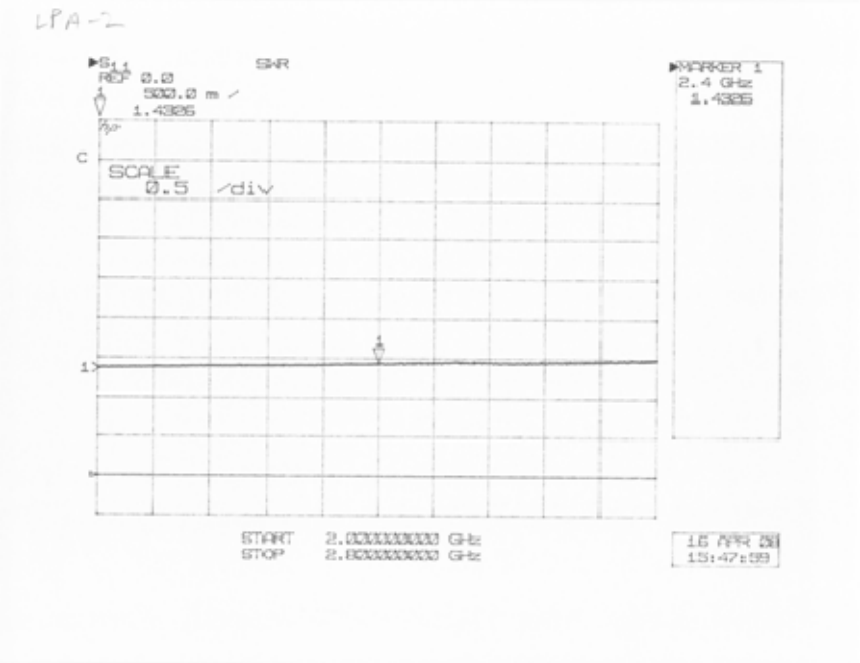

Figure 171. LPA2; S11

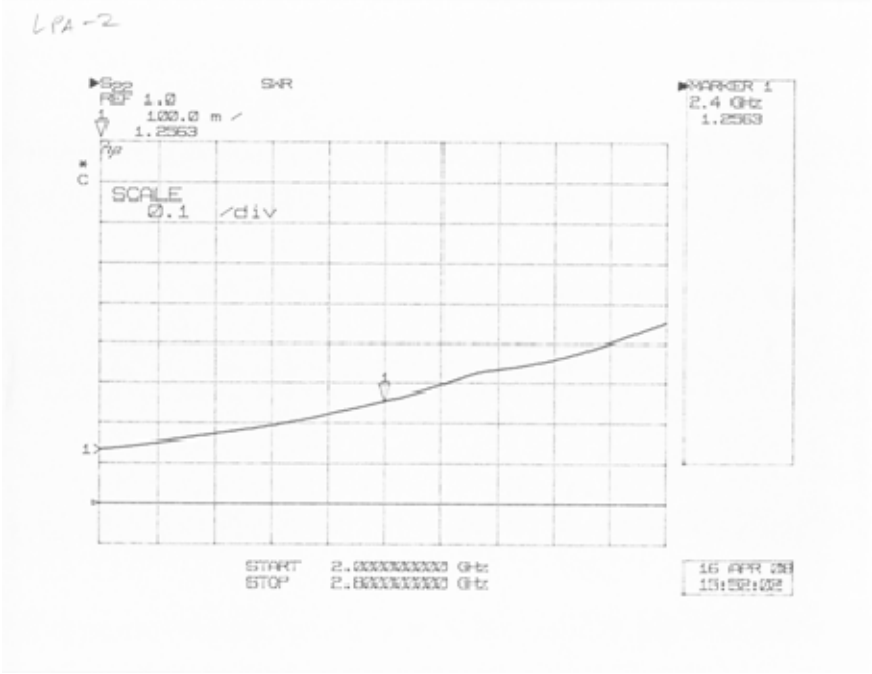

Figure 172. LPA2; S22

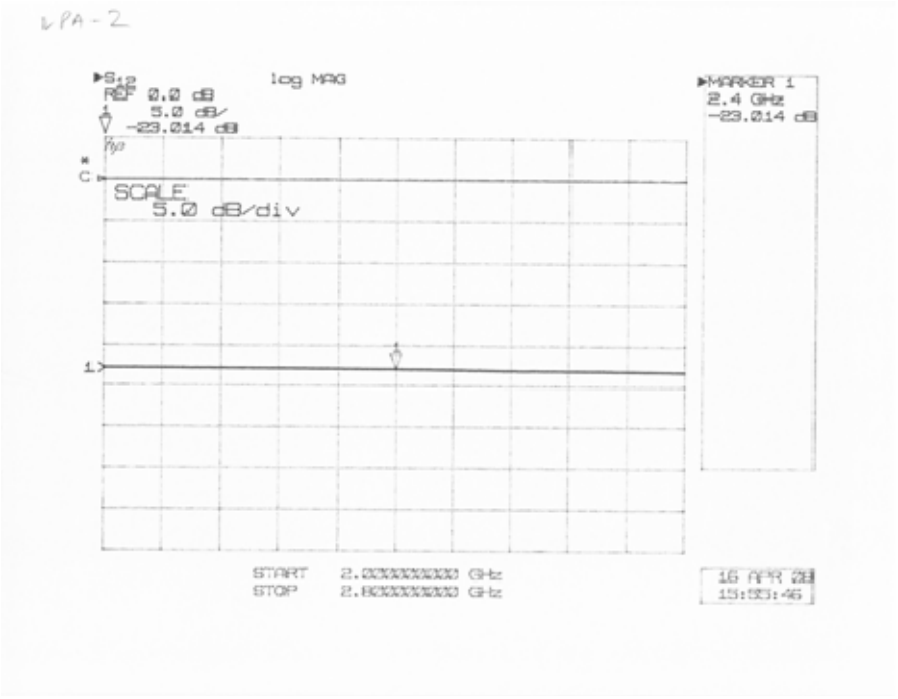

Figure 173. LPA2; S12

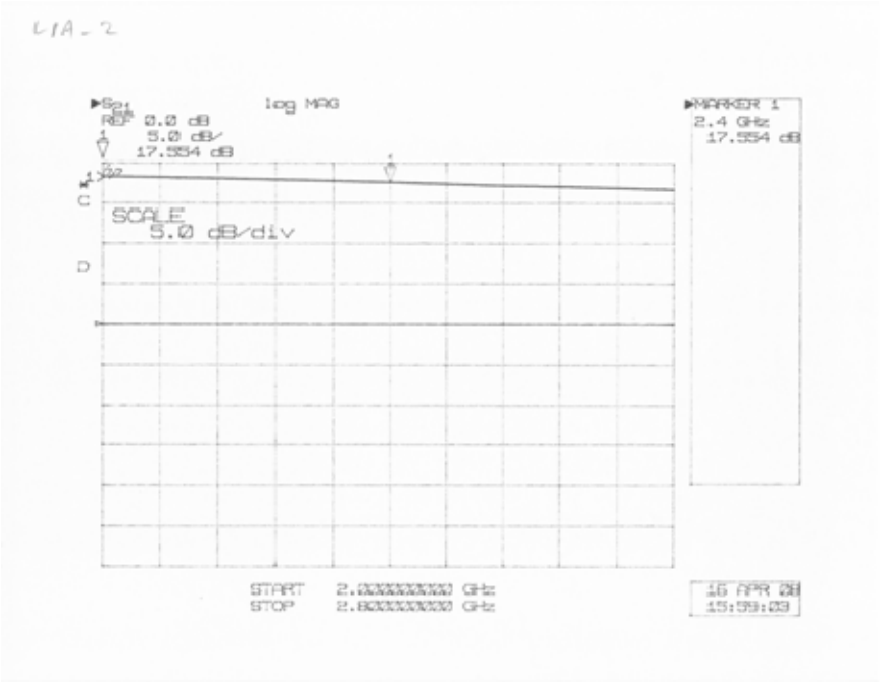

Figure 174. LPA2; S21

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